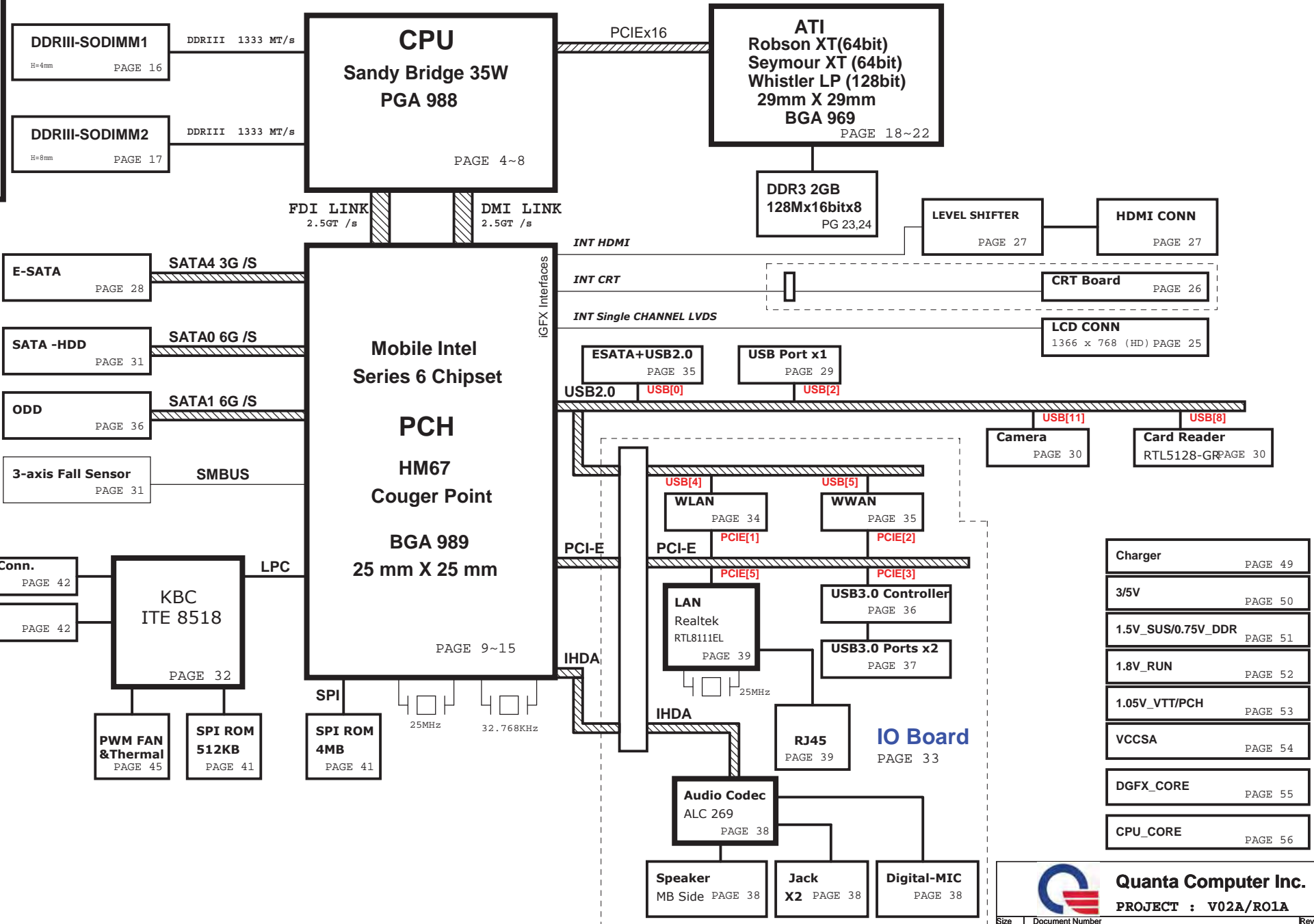


V02A/R01A DIS BLOCK DIAGRAM

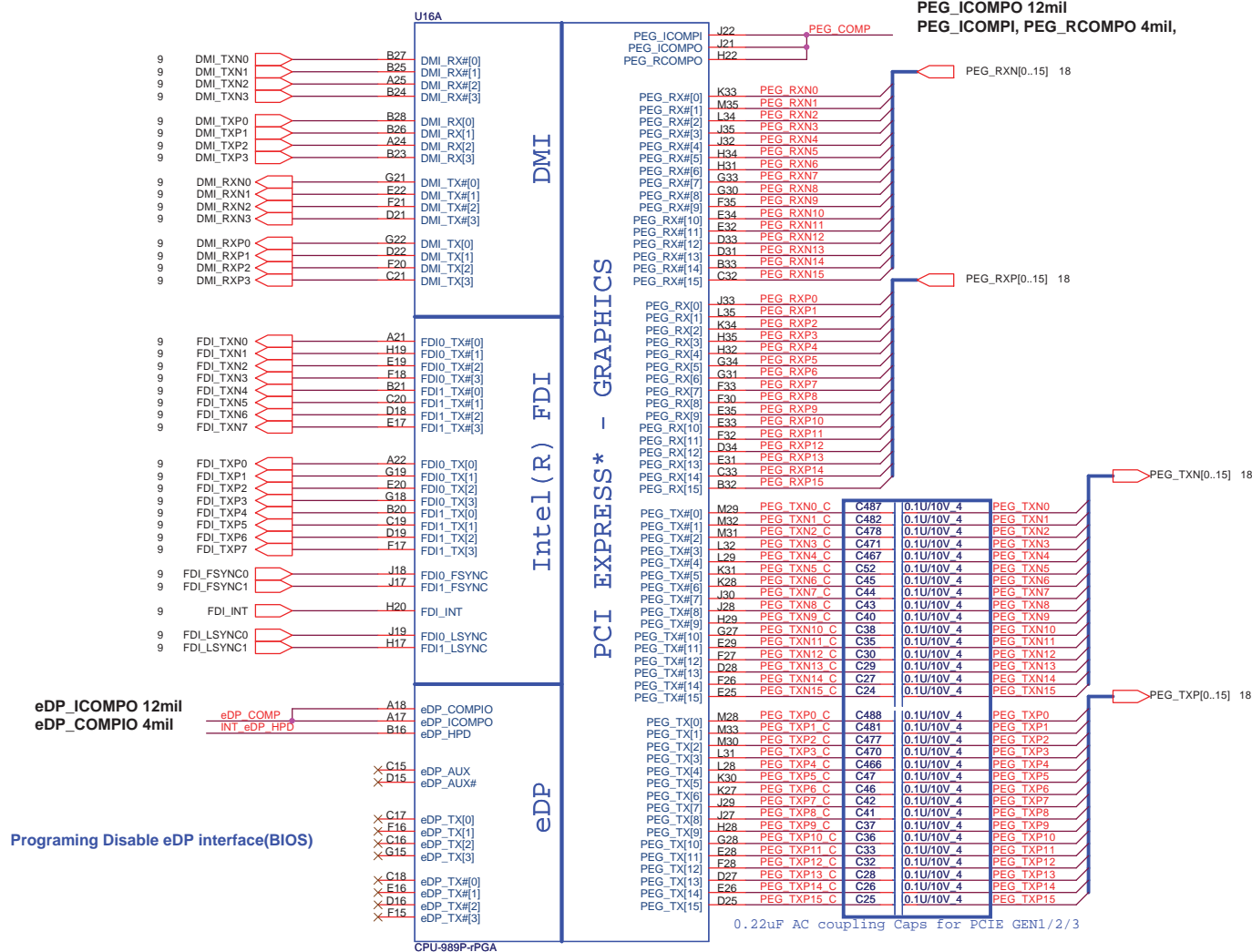
- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND
- LAYER 8 : BOT



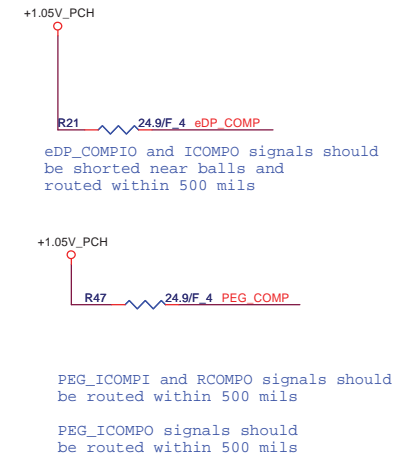
power State					
S0					
S1					
S3					
S4/S5 AC					
S4/S5 DC Only					
AC/DC No Exist					

SMBCLK SMBDATA								
SMB_CLK_ME1 SMB_DAT_ME1								
AB1A_CLK AB1A_DATA								

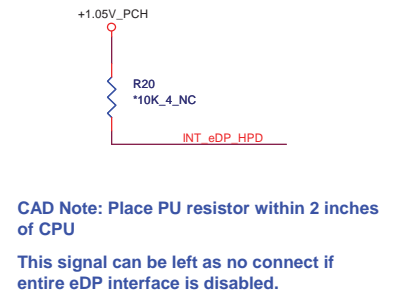
Sandy Bridge Processor (DMI, PEG, FDI)



DP & PEG Compensation



eDP Hot-plug (Disable)



SNB_IVB# N.A at SNB EDS #27637 0.7v1

12 H_SNB_IVB# H_SNB_IVB# C26

32 H_CPUDET# AN34

32 PECL_EC R73 43_4 AN33

32,44,47 IMVP7_PROCHOT# R77 56/J 4 H_PROCHOT# AL32

14 PM_THRMTRIP# AN32

9 H_PM_SYNC AM34

14 H_PWRGOOD AP33

UNCOREPWRGOOD

SM_DRAMPWROK V8

RESET#

CPU_PLTRST# R81 75_4 NC

CPU_PLTRST# R82 43/J 4 NC CPU_PLTRST# R AR33

SM_DRAMPWROK

SM_DRAMPWROK

SM_DRAMPWROK

SM_DRAMPWROK

SM_DRAMPWROK

SM_DRAMPWROK

SM_DRAMPWROK

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SM_DRAMPWROK

SM_DRAMPWROK

U16B

PROC_SELECT#

SKTOCC#

CATERR#

PECI

PROCHOT#

THERMTRIP#

PM_SYNC

UNCOREPWRGOOD

SM_DRAMPWROK

RESET#

SM_DRAMPWROK

SM_DRAMPWROK

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SM_DRAMPWROK

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SM_DRAMPWROK

MISC

THERMAL

PWR MANAGEMENT

CLOCKS

DDR3 MISC

JTAG & BPM

BCLK

BCLK#

DPLL_REF_CLK

DPLL_REF_CLK#

SM_DRAMRST#

SM_RCOMP[0]

SM_RCOMP[1]

SM_RCOMP[2]

PRDY#

PREQ#

TCK

TMS

TRST#

TDI

TDO

DBR#

BPM#[0]

BPM#[1]

BPM#[2]

BPM#[3]

BPM#[4]

BPM#[5]

BPM#[6]

BPM#[7]

A28

A27

A16

A15

A14

A13

A12

A11

A10

A9

A8

A7

A6

A5

A4

A3

A2

A1

A0

A-1

A-2

A-3

A-4

A-5

A-6

A-7

A-8

A-9

A-10

A-11

A-12

CLK_CPU_BCLKP

CLK_CPU_BCLKN

CLK_DP_P

CLK_DP_N

CLK_DP_P

CLK_DP_N

CLK_DP_P

CLK_DP_N

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SM_RCOMP_0, SM_RCOMP_1 20mil
SM_RCOMP_2 15mil,

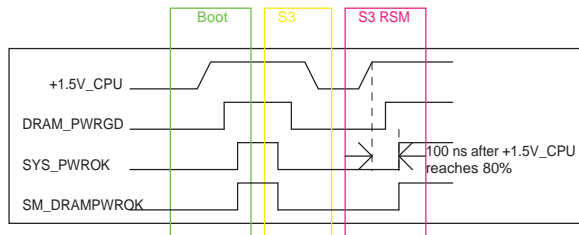
XDP_TMS R333 51/J 4
XDP_TDI R328 51/J 4
XDP_TDO R334 51/J 4
IMVP7_PROCHOT# R76 62/J 4
XDP_TCLK R335 51/J 4

XDP_DBRST# use a 1k pull-up to 3.3V_S
TRST# use a 51ohm pull down.

When MP, JTAG PU/PD resistor
can be removed?
Need to confirm with Intel

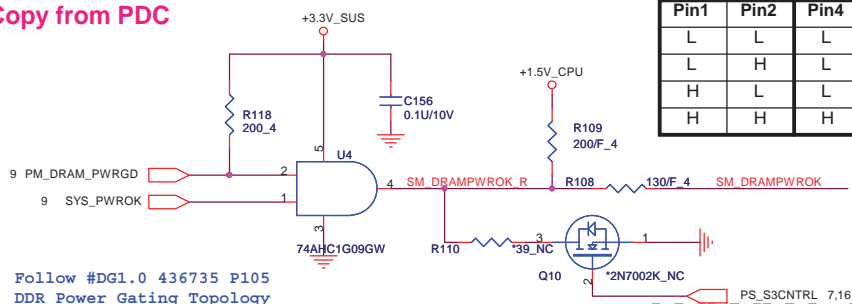
CPU_PLTRST	R497,R126	U19,C544,R81,R82
Option1	POP	NC
Option2	NC	POP

IN	OUT
L	L
H	High-Z



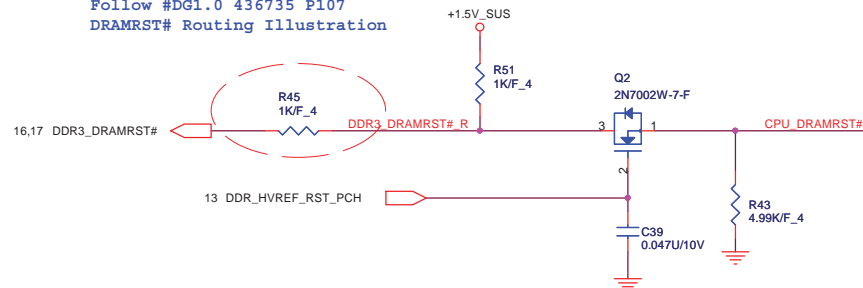
Change OD part same with PDC

Copy from PDC



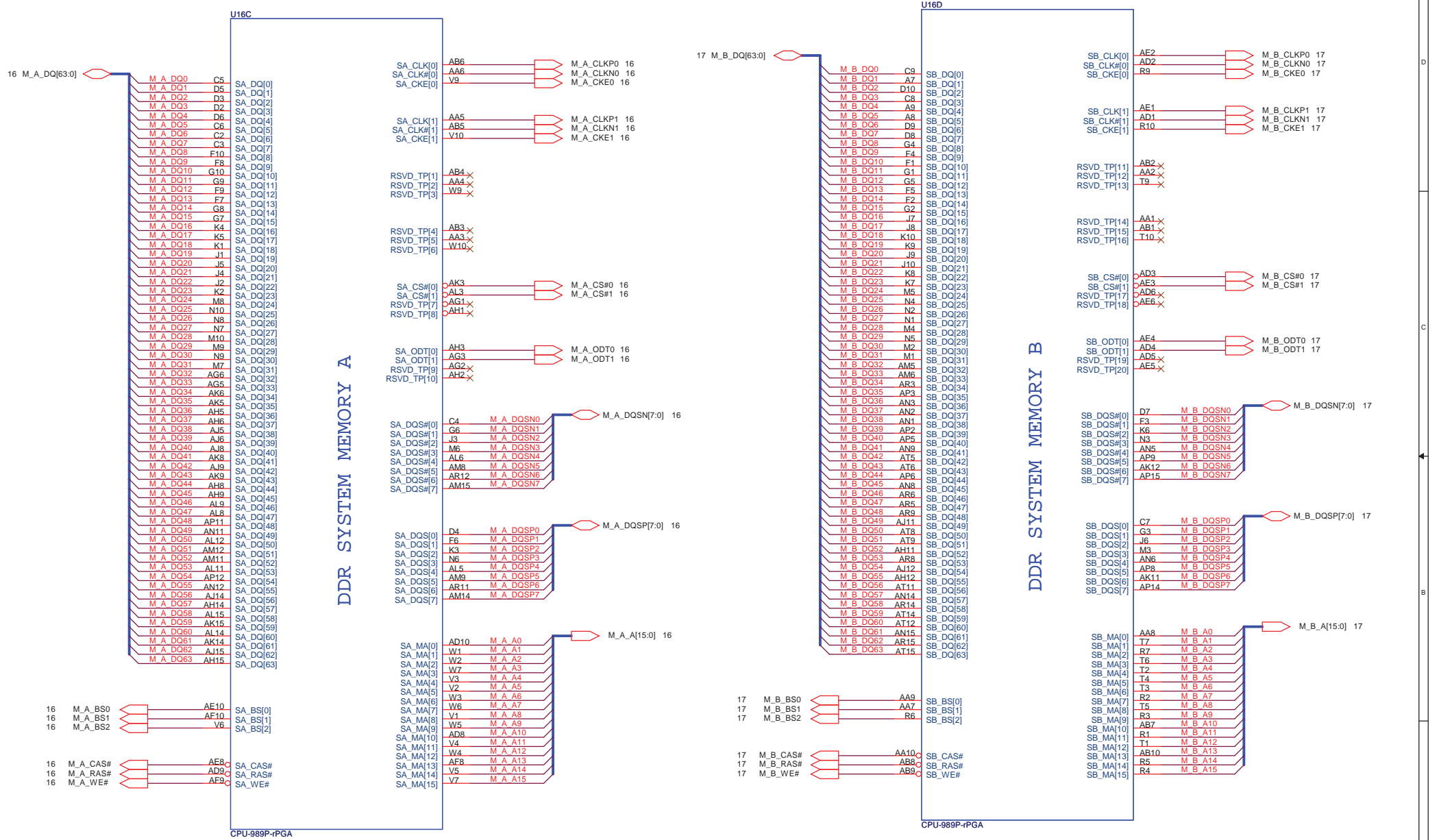
Follow #DG1.0 436735 P105
DDR Power Gating Topology

Follow #DG1.0 436735 P107
DRAMRST# Routing Illustration



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PROJECT : V02A/R01A

Size	Document Number	Rev
	Sandy Bridge 2/5	1A
Date:	Wednesday, January 19, 2011	Sheet 5 of 61



Quanta Computer Inc.

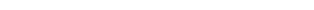
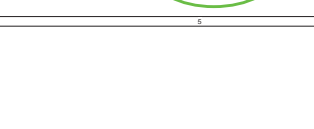
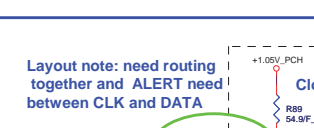
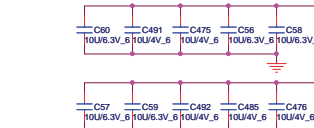
PROJECT : V02A/R01A

Size	Document Number	Rev
	Sandy Bridge 3/5	1A
Date:	Wednesday, January 19, 2011	Sheet 6 of 61

CPU VTT
SNB 35W:8.5A
10F x12

POWER

CPU Core Power
SNB 35W:55A
10uF x 24





```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

The CFG signals have a default value of '1' if not terminated on the board.

CFG2 R106 1K/F 4



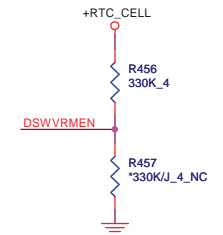
PROJECT : V02A/R01A

ent Number

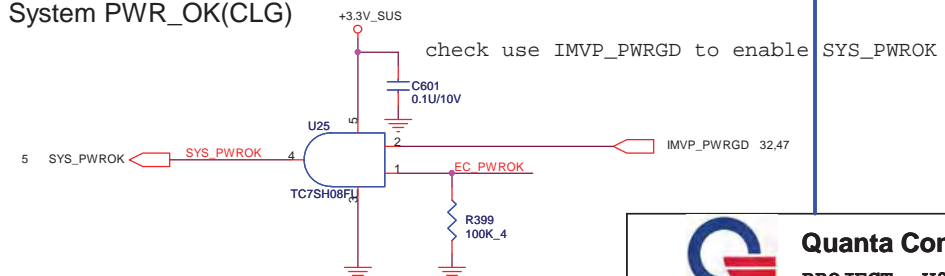
Size	Document Number	Rev
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	Sandy Bridge 5/5	1A
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Date: Wednesday, January 19, 2011 Sheet 8 of 61



On Die DSW VR Enable
High = Enable (Default)
Low = Disable

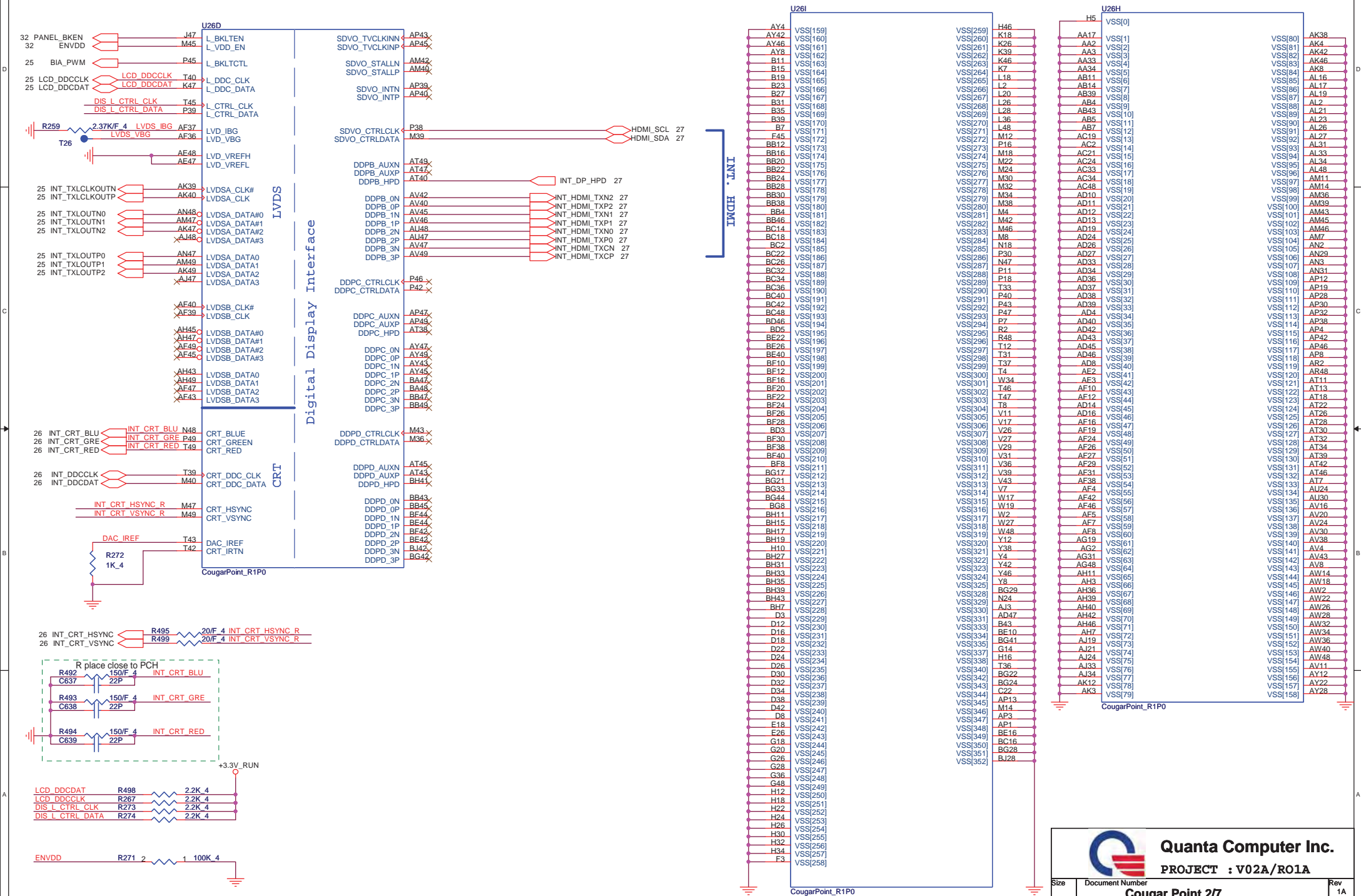


PROJECT : V02A/R01A

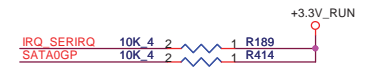
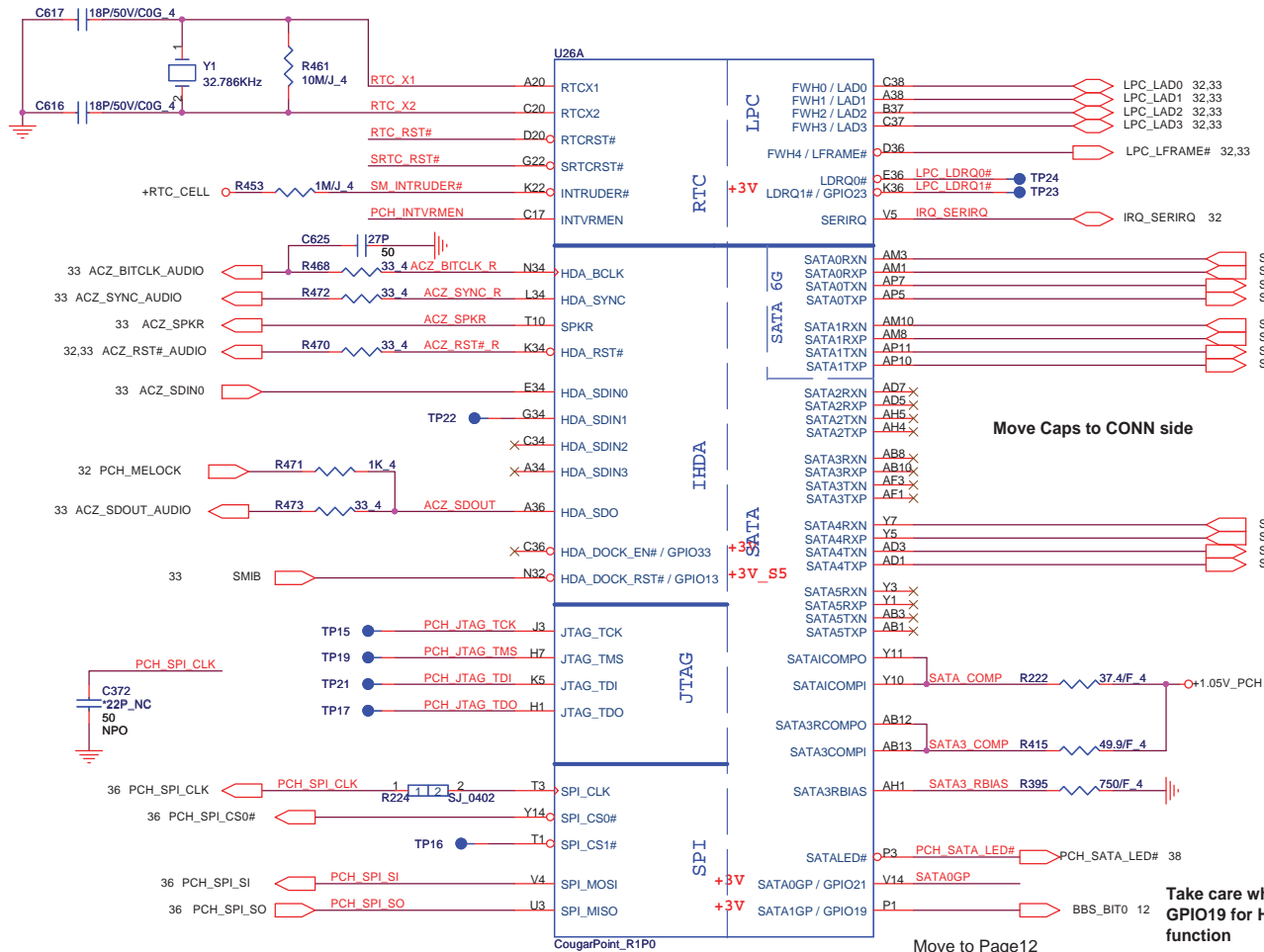
Cougar Point 1/7

Size	Document Number	Rev
	Cougar Point 1/7	1A
Date:	Wednesday, January 19, 2011	Sheet 9 of 61

Cougar Point (GND)

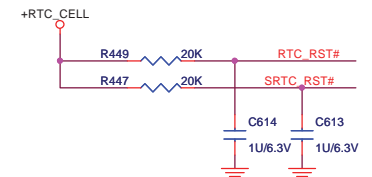
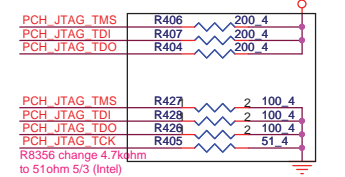


Cougar Point (HDA, JTAG, SATA)



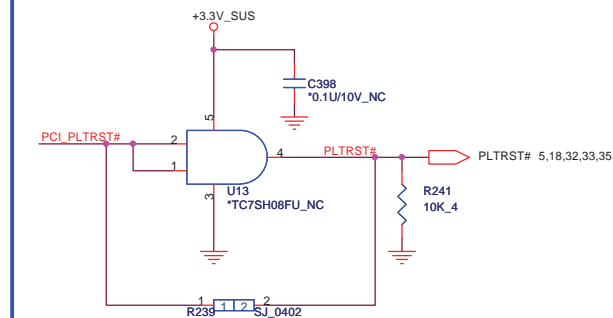
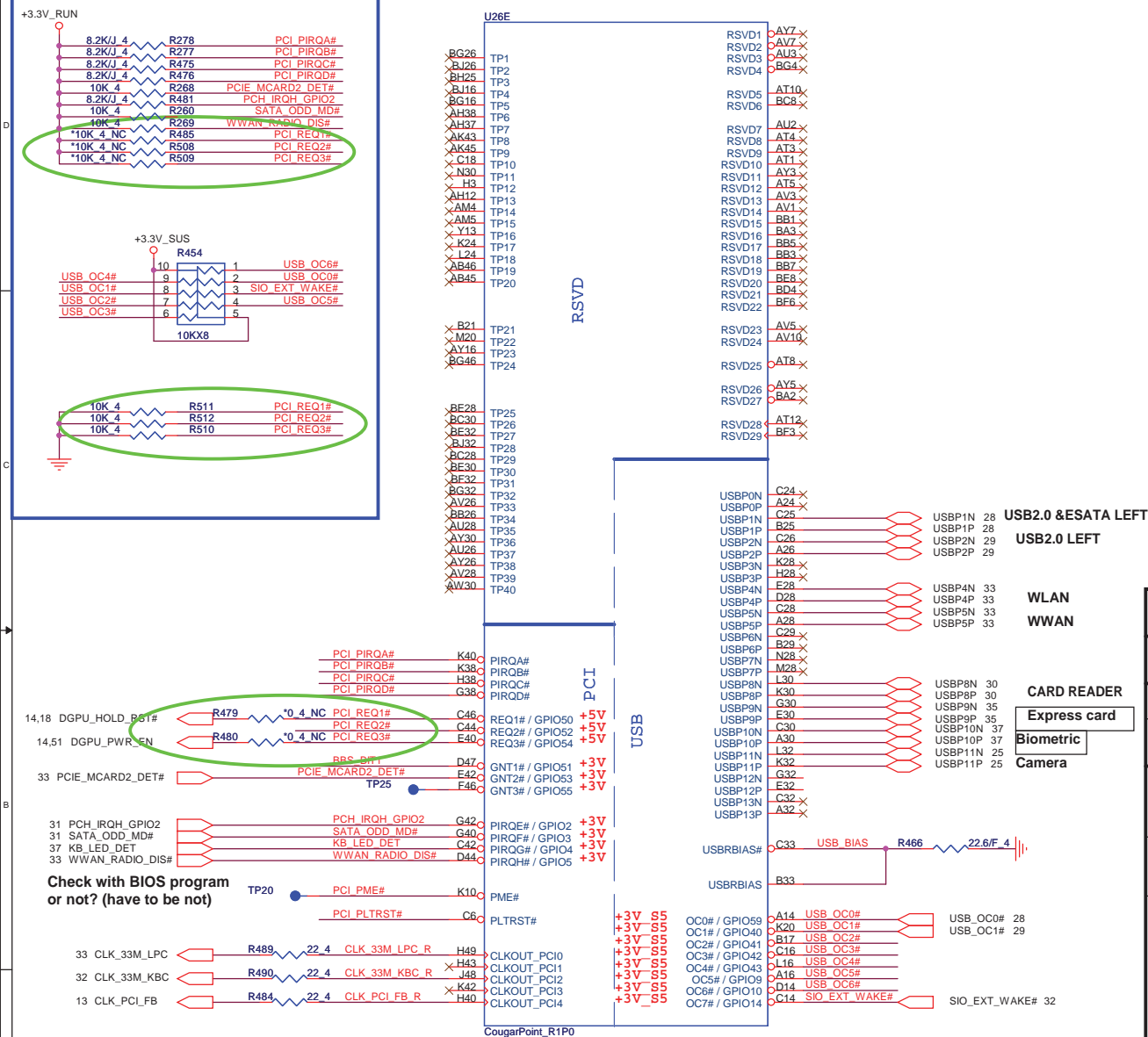
PCH JTAG Debug (CLG)

5% fine (Intel), 210->200 (PDDG, Intel) MP remove(Intel)



PCH Strap Table

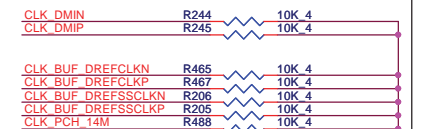
Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_SUS ○ R413 1K 4 NC ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS ○ R474 1K 4 NC ACZ_SDOOUT
Del 0510			Remove SPI_MOSI from PCH strapping, HR_C/L_v0.91	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL ○ R455 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS ○ R469 1K 4 ACZ_SYNC_R



Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>Bit 0</th><th>Bit 1</th><th>Boot Location</th></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										
<div><div><div>BBS_BIT1</div><div>R496</div><div></div><div>*1K 4 NC</div></div><div><div>11 BBS_BIT0</div><div></div><div>R394</div><div></div><div>*1K 4 NC</div><div></div></div></div> <div>Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]</div>												
DF_TV5	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm									
<div><div><div><div>R420</div><div></div><div>2.2K 4</div></div><div><div>R424</div><div>2</div><div></div><div>1</div><div>SJ_0402</div></div></div><div><div></div><div>*1.8V_RUN</div></div><div><div>DF_TV5</div><div>14</div></div><div><div>H_SNB_IVB#</div><div>5</div></div></div> <div>CheckList_1.0 p58; HR_v1.0 p450</div>												



Quanta Computer Inc.
PROJECT : V02A/R01A



Port R1P0	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 / GPIO64	• 33 / 27 / 48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 / GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC /48/24 MHz
CLKOUTFLEX2 / GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 / GPIO67	• 27/14.318 MHz output to SIO/EC/24 MHz (Default)

**Quanta Computer Inc.**

PROJECT : V02A/R01A

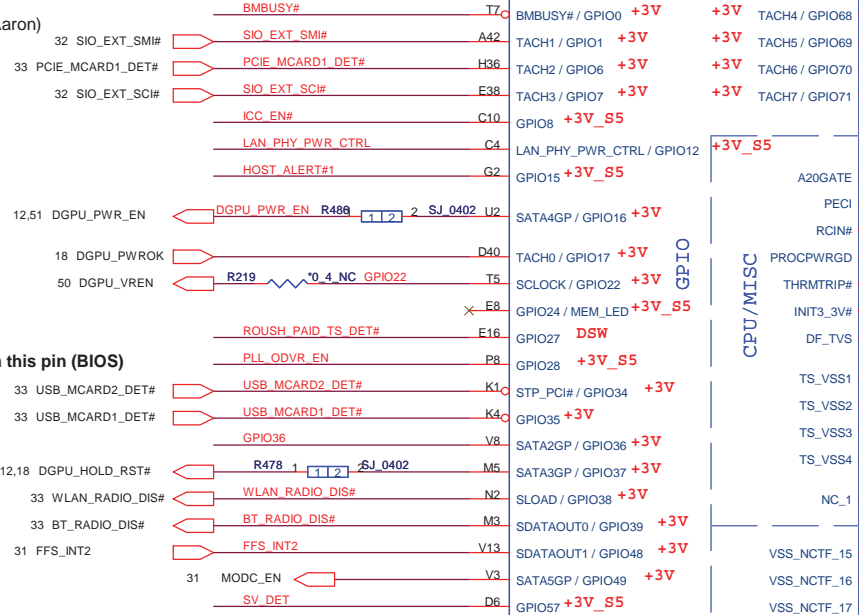
Cougar Point 5/7

Size	Document Number	Rev
	Cougar Point 5/7	1A
Date:	Wednesday, January 19, 2011	Sheet 13 of 61

Cougar Point (GPIO,VSS_NCTF,RSVD)

Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

change to GPIO14 (Aaron)



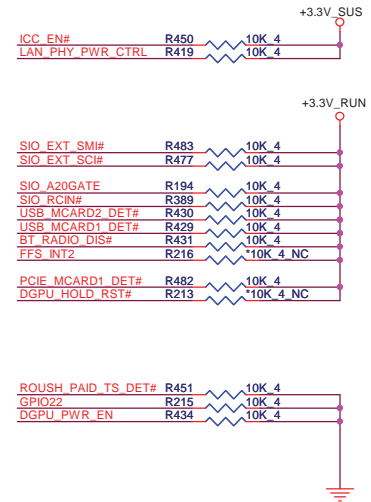
DO NOT program this pin (BIOS)

CPU/MISC

NCTF

Check When Symbol Update (OK)

GPIO Pull-up/Pull-down(CLG)



Can be del



Have to Reserve

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

MFG-TEST



SGPIO Confirm with Intel

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.



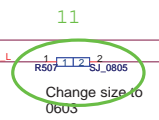
BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 KΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm pull-up for validation purpose

DMI TERMINATION VOLTAGE OVERRIDE
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

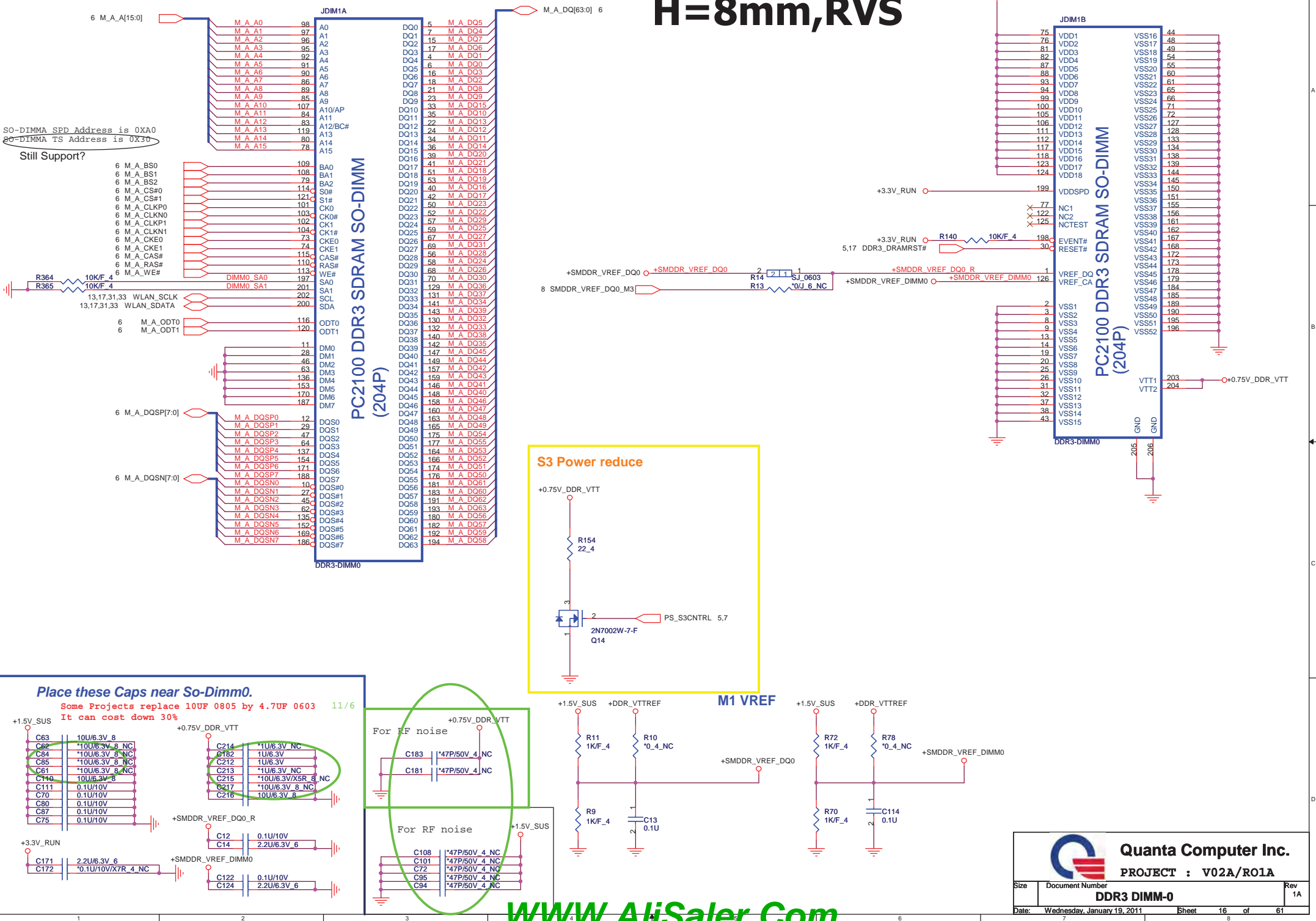


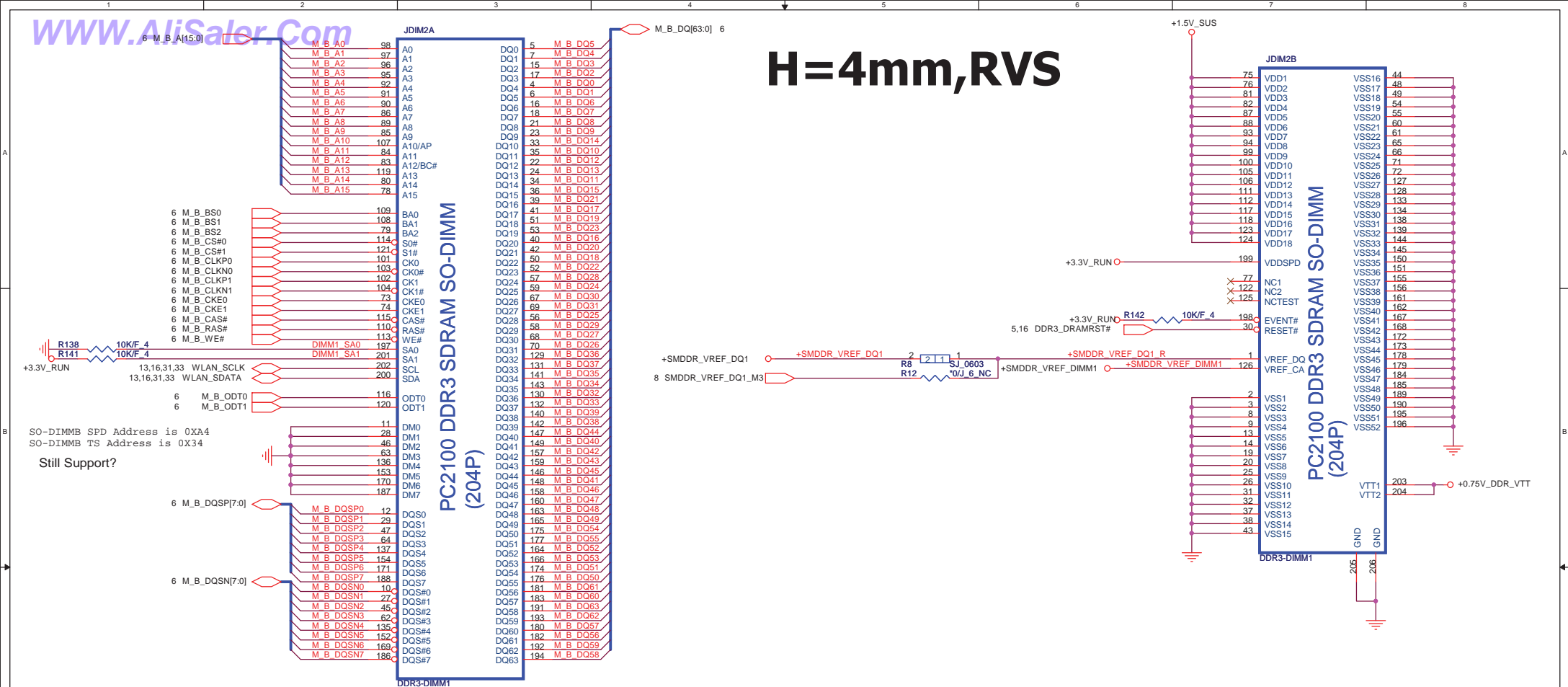
Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	Cougar Point 6/7	1A
Date:	Wednesday, January 19, 2011	Sheet 14 of 61

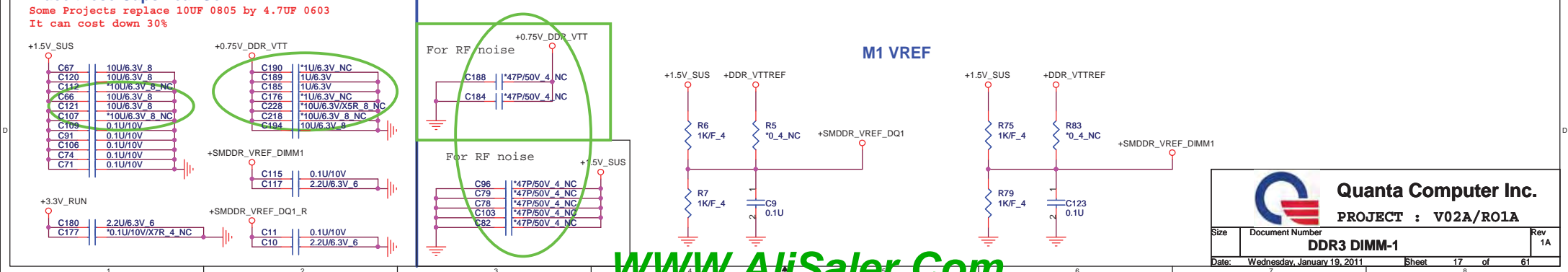


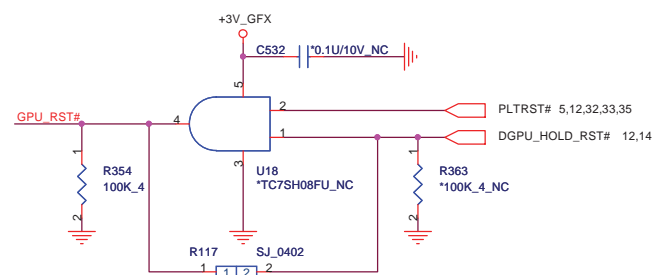
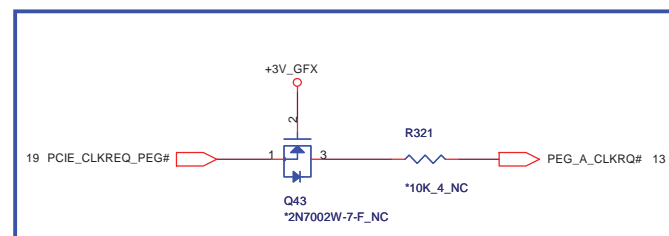
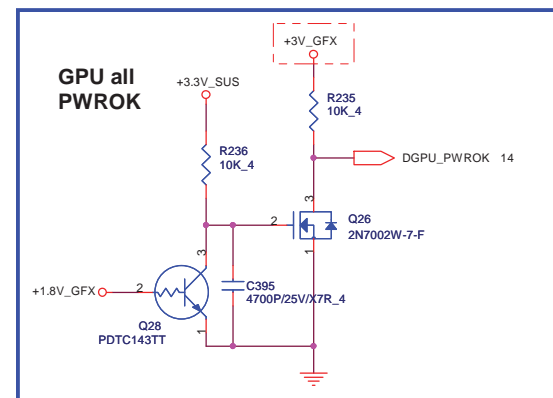
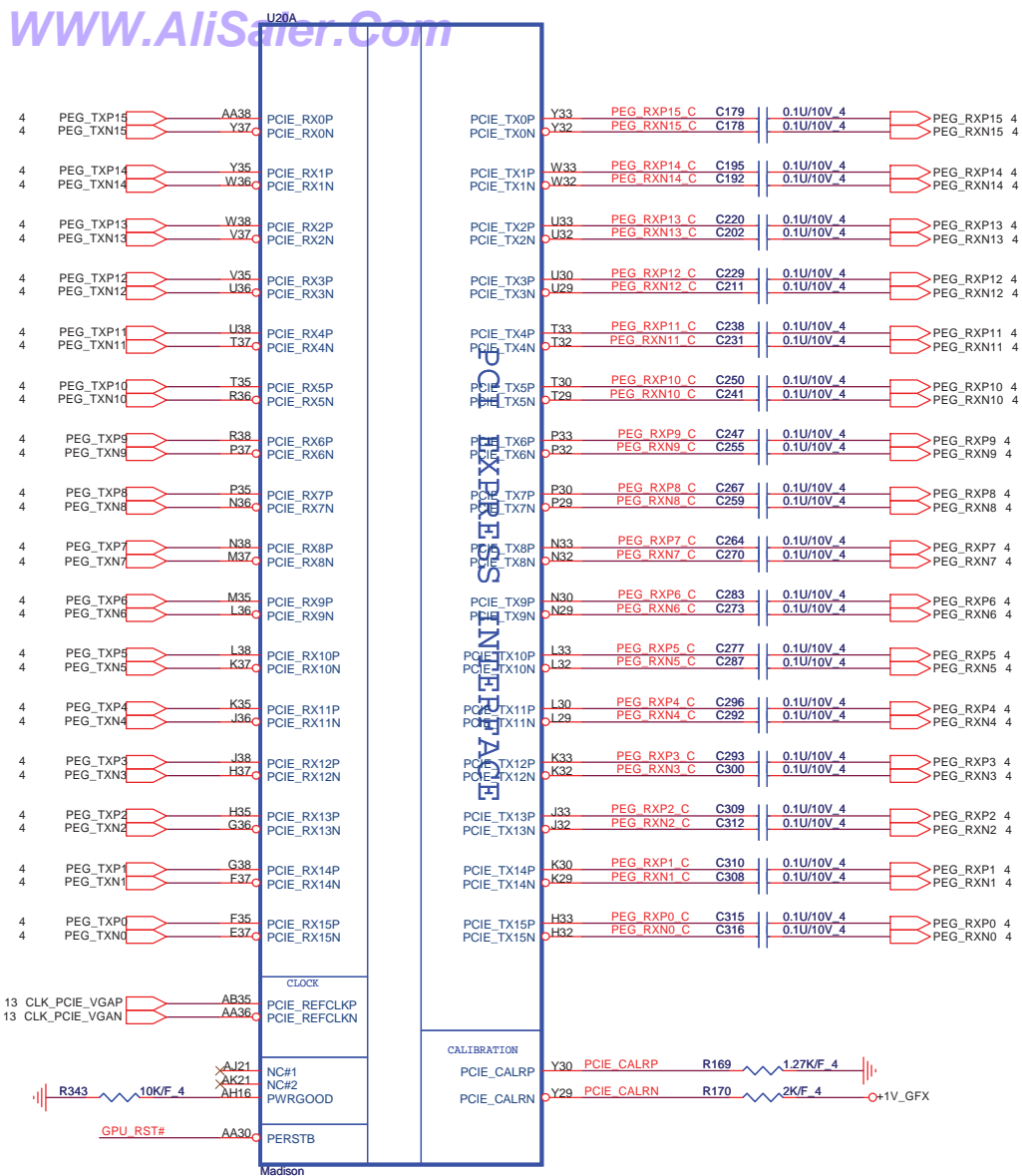
H=8mm,RVS





Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%



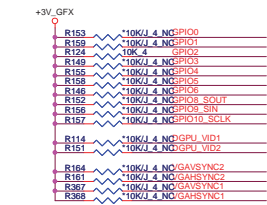


WWW.AliSaler.Com

STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	0
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	1
GPIO_5_AC_BATT (M96-M2)	GPIO5	1 = AC (Performance mode) 0 = Battery saving mode	0
VGA_DIS	GPIO9	0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGA_VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	00
VIP_DEVICE_STRAP_EN	BIOS_ROM_EN	VIP Device Strap Enable 0 = Disable ; 1 = Enable	0

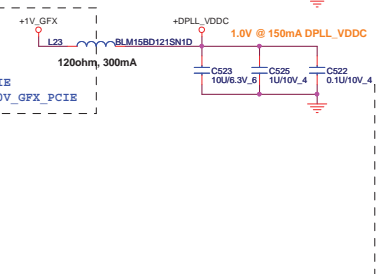
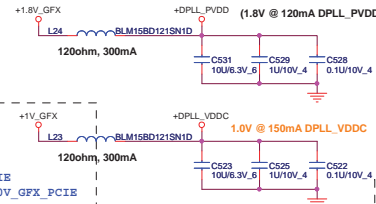
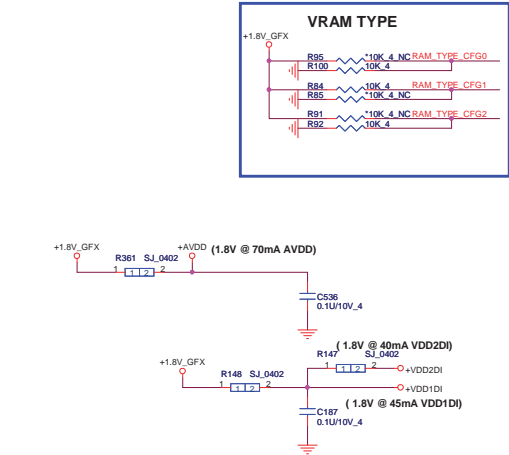
APERTURE SIZE

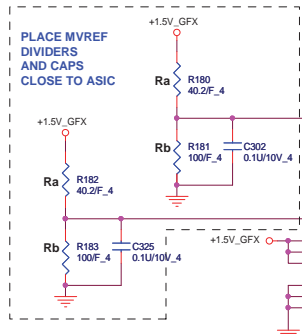
MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG2	CFG1	CFG0	GPIO11
128MB	0	0	0	1
256MB	0	0	0	1
64MB	0	1	0	



Memory Straps	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Vendor PN	Support GPU
900MHz Samsung 1GB(128M*16*4pcs)	0	0	1	AKD5MGWT507	K4W2G1646C-HC11	For Robson XT (Only Channel B)
900MHz Hynix 1GB(128M*16*4pcs)	0	1	0	AKD5MGWTW06	H5TQ2G63BFR-11C	For Robson XT (Only Channel B)

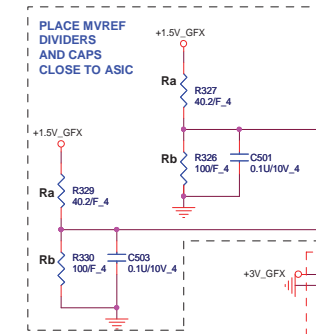
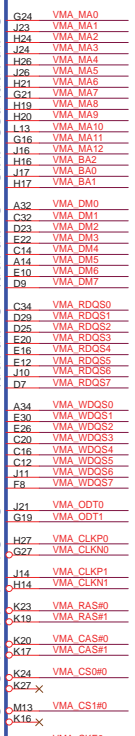
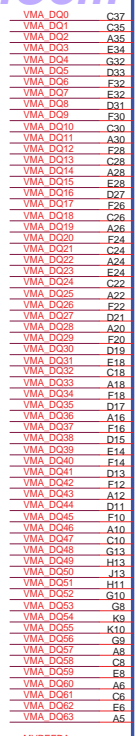
Memory Straps	RAM_TYPE_CFG2	RAM_TYPE_CFG1	RAM_TYPE_CFG0	Quanta PN (QuantaBuy)	Vendor PN	Support GPU
900MHz Samsung 1GB(64M*16*8pcs)	0	0	1	AKD5LGH7505	K4W1G1646E-HC11	For Whisler-LP
900MHz Hynix 1GB(64M*16*8pcs)	0	1	0	AKD5LZWTW07	H5TQ1G63BFR-11C	For Whisler-LP
900MHz Samsung 1GB(64M*16*8pcs)	1	0	0	AKD5EGGT500	K4W1G1646G-BC11	For Whisler-LP



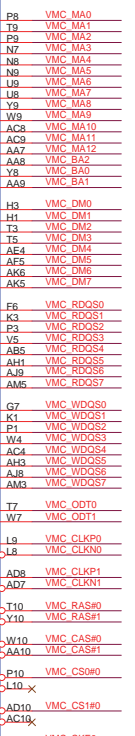
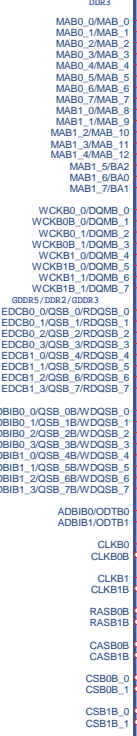
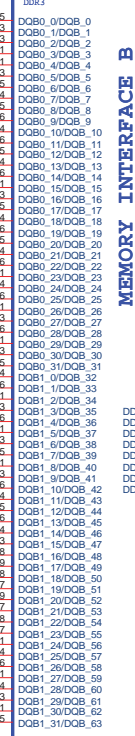
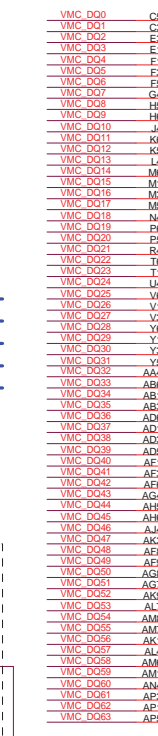


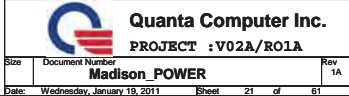
	GDDR3	DDR3
MVDDQ	1.8V	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

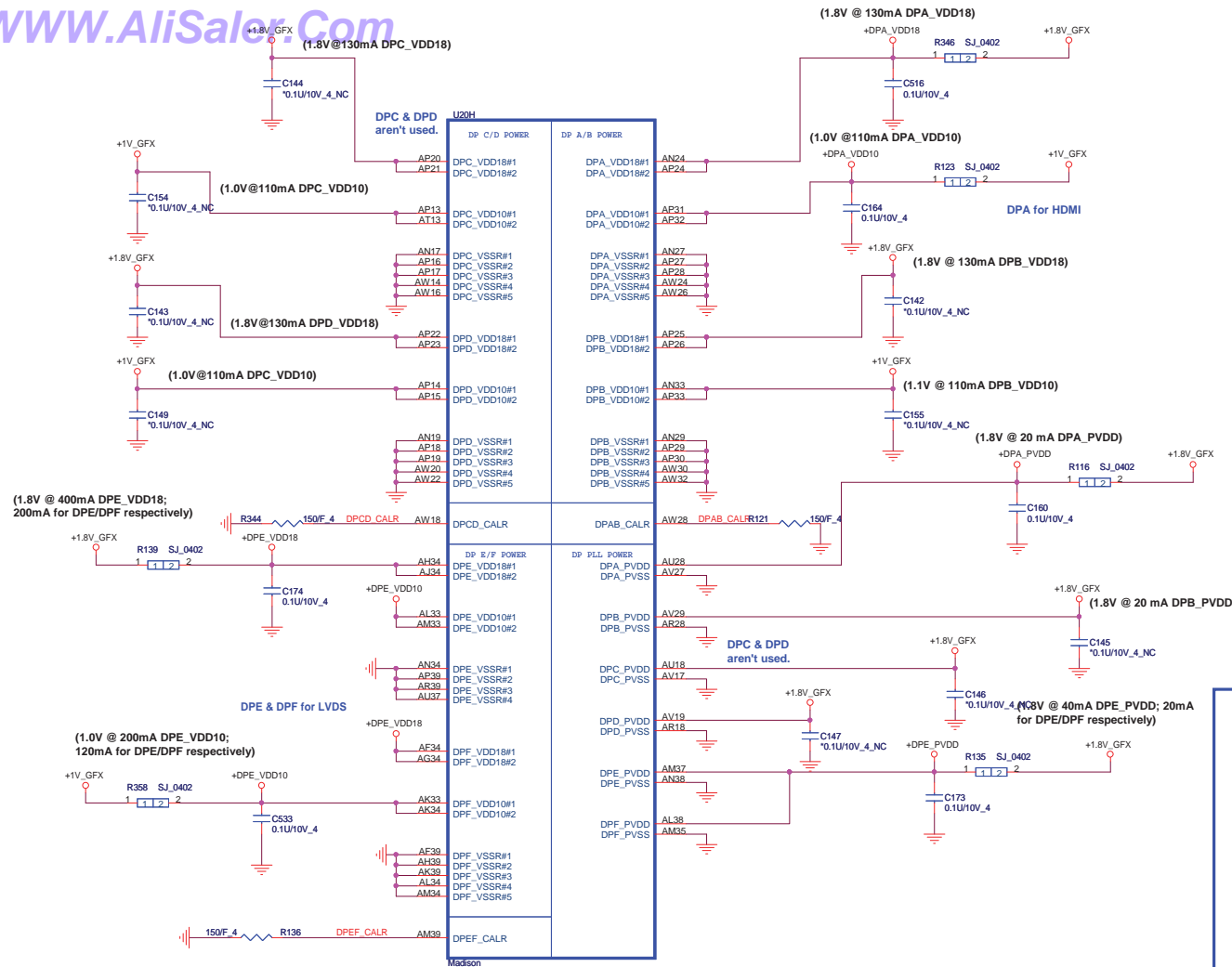
03/02 correct table.



03/01 un-stuff







GPU Power Rail List

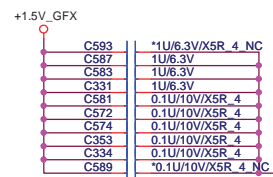
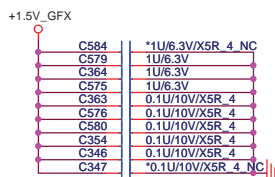
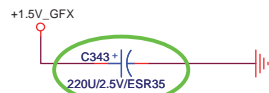
+1V_GFX=>
 +DPA_VDD10
 +SPV10
 +DPE_VDD10
 +DPLL_VDDC
 +PCIE_VDDC

+1.8V_GPU=>
 +A2VDDQ
 +AVDD
 +DPA_PVDD
 +DPA_VDD18
 +DPE_PVDD
 +DPE_VDD18
 +DPLL_PVDD
 +MPV18
 +PCIE_PVDD
 +PCIE_VDDR
 +SPV18
 +TSVDD
 +VDD1DI
 +VDD2DI
 +VDD_CT
 +VDDR4

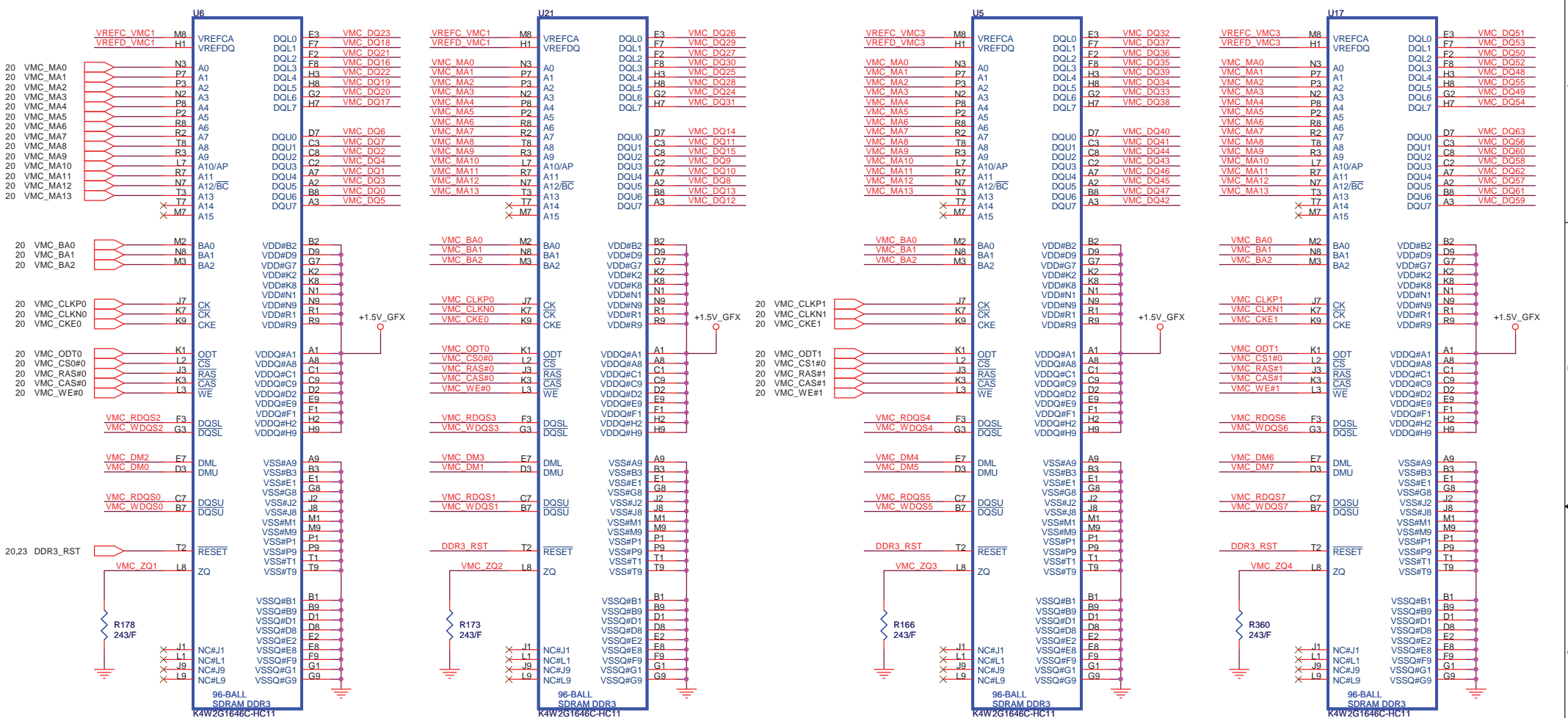
GPU Power-on sequence

- 1 => +3V_GFX
- 2 => +VCC_DGFX_CORE
- 3 => +1V_GFX
- 4 => +1.5V_GFX
- 5 => +1.8V_GFX
- 6 => dGPU_PWROK

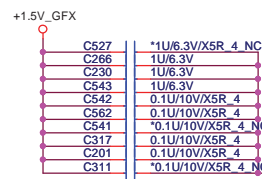
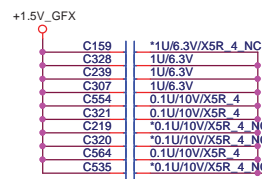
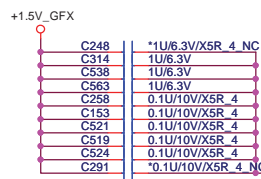
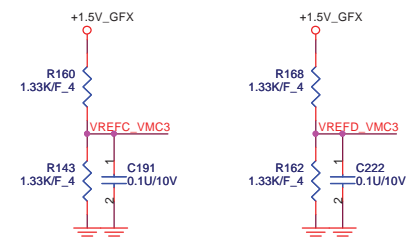
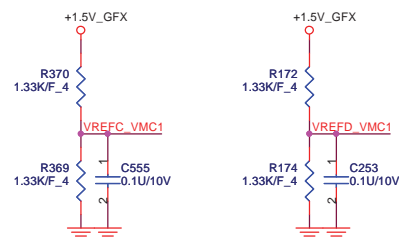
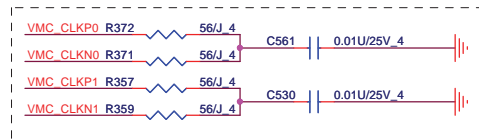
WWW.AliSaler.Com

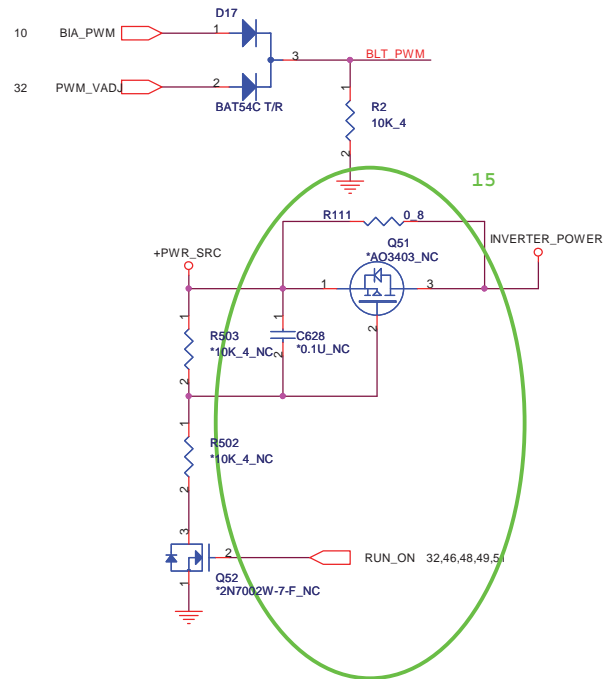
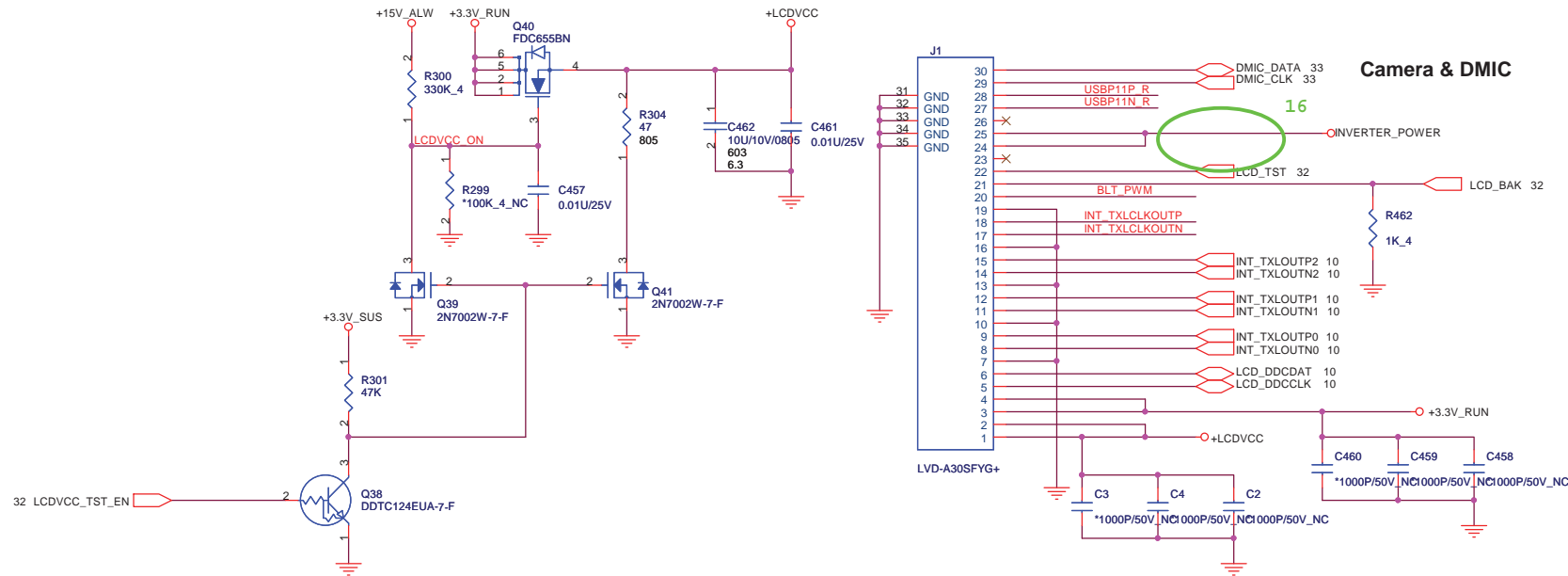


A diagram showing a 4x4 grid of hexagons. The hexagons are arranged in four rows and four columns. The hexagons in the first three columns are red, and the hexagons in the fourth column are blue. Four blue lines extend horizontally from the right side of the hexagons in the first three rows, and a blue line extends from the bottom of the hexagon in the fourth row.

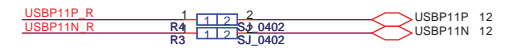
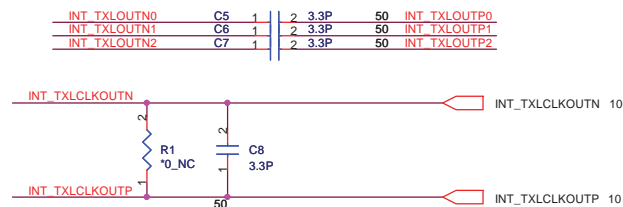


Placement has to be close to VRAM



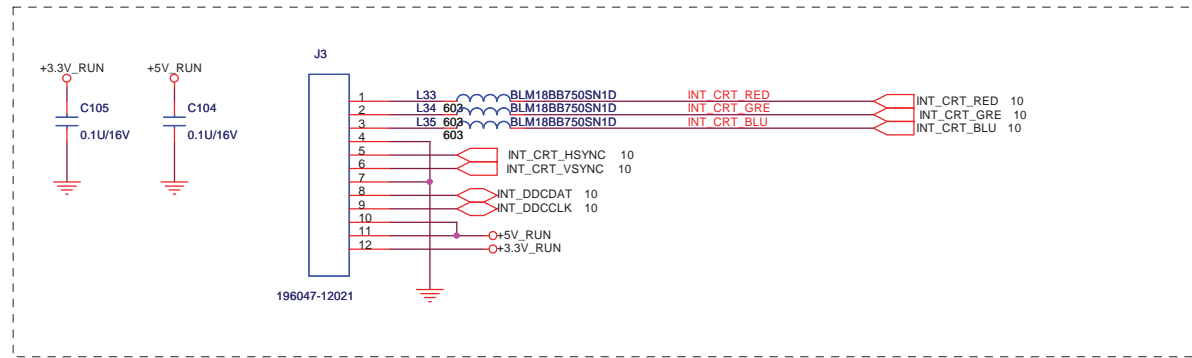


Shunt capacitors on LVDS for improving WWAN.

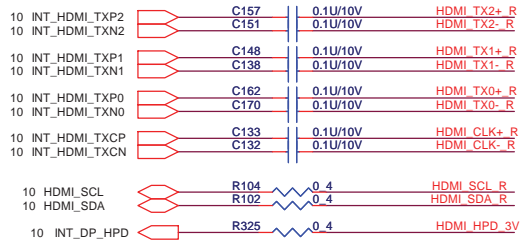


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PROJECT : V02A/R01A

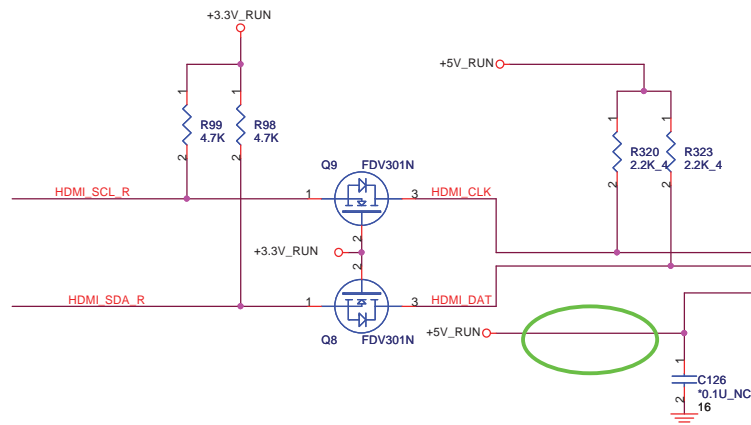
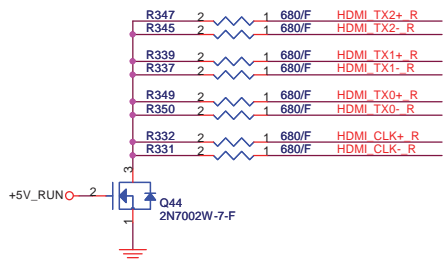
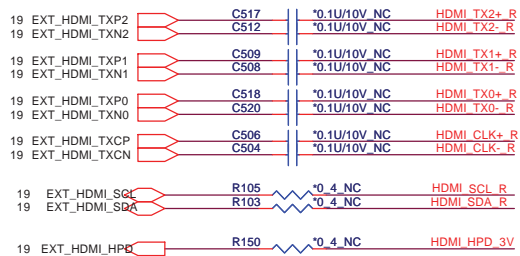
Size	Document Number	Rev
	LVDS CONN	1A
Date:	Wednesday, January 19, 2011	Sheet 25 of 61



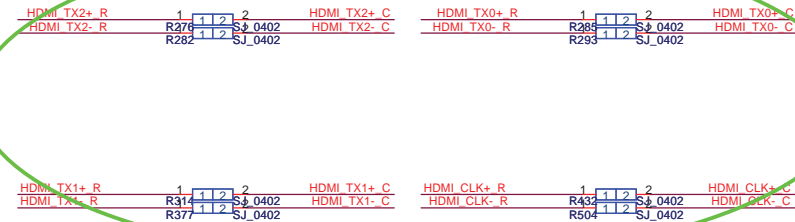
UMA HDMI



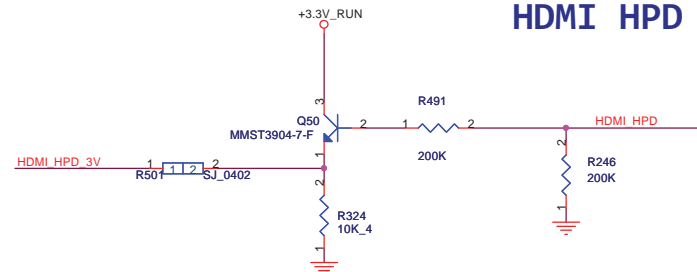
DIS HDMI



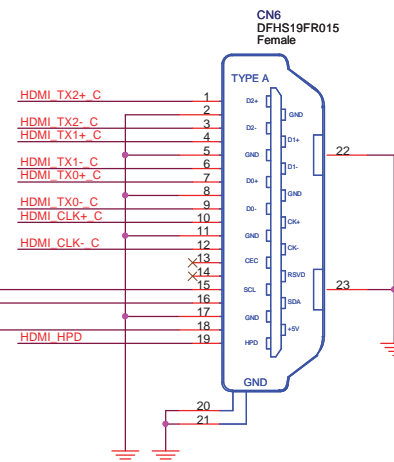
Reserve for EMI and close to HDMI CONN



HDMI HPD



HDMI Conn.



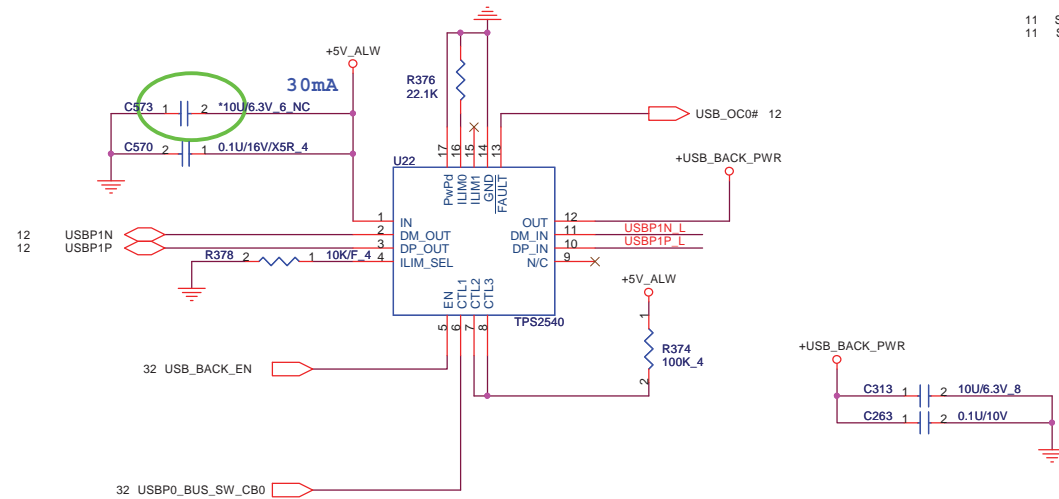
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PROJECT : V02A/R01A

Size	Document Number	Rev
	HDMI CONN	1A
Date:	Wednesday, January 19, 2011	Sheet 27 of 61

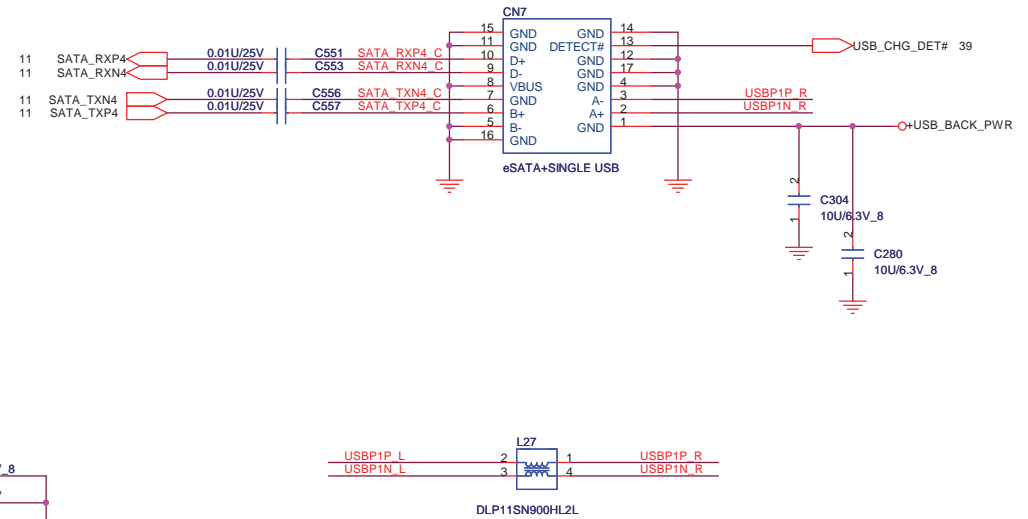
ESATA + USB Conn + Power share

S3/S5 USB charging circuit

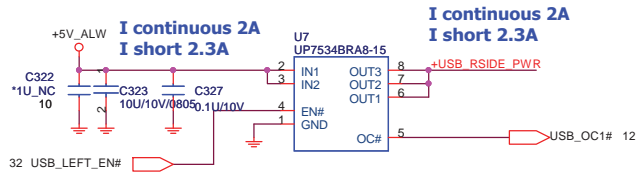


USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

	R8224	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

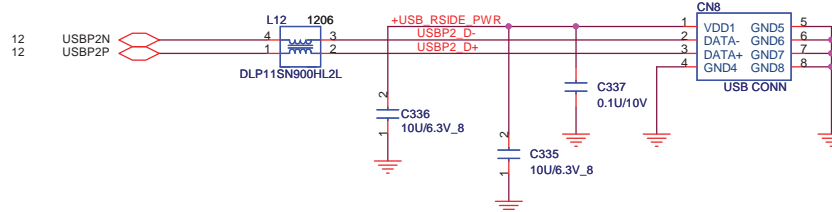
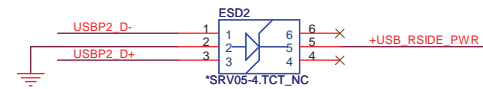


UPI power switch



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

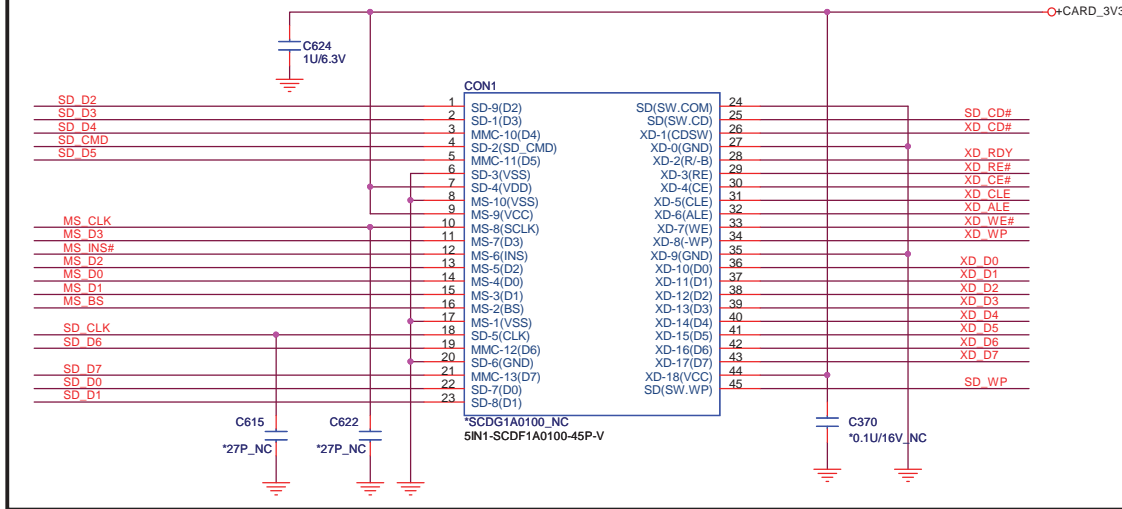
Place ESD diodes as close as USB connector.



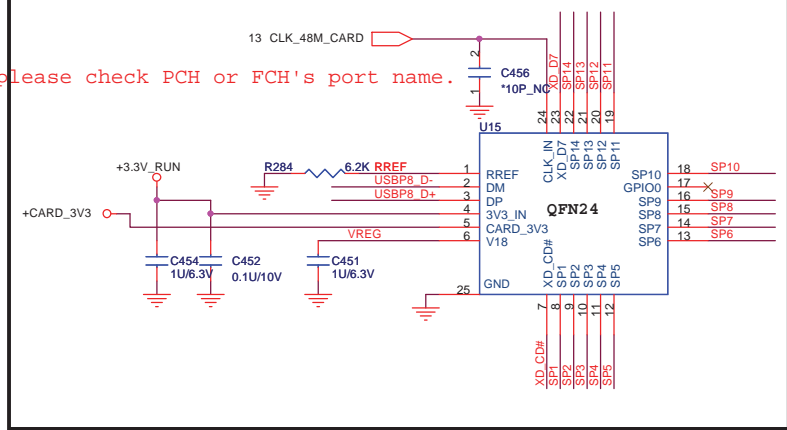
Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	USB 2.0	1A
Date:	Wednesday, January 19, 2011	Sheet 29 of 61

Inspiron

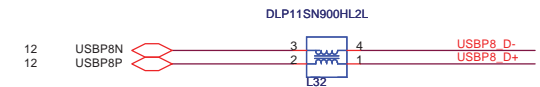


please check PCH or FCH's port name.

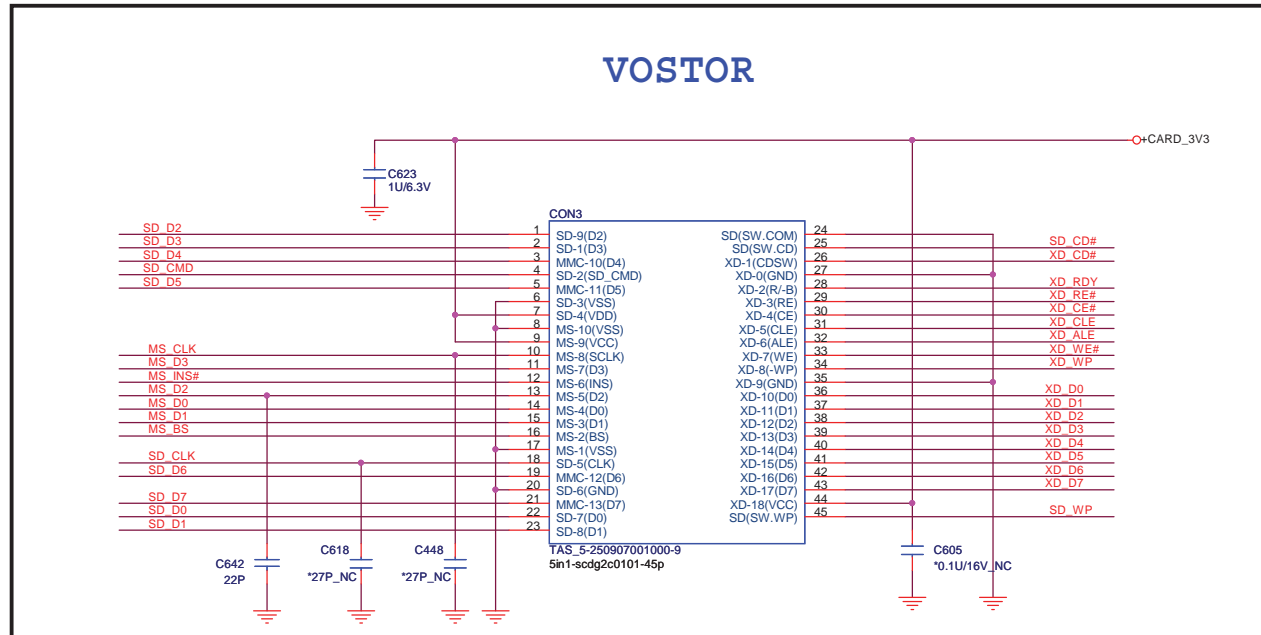


SP1	XD RDY	SD WP	MS CLK
SP2	XD RE#	SD D1	MS INS#
SP3	XD CE#	SD D0	MS D7
SP4	XD CLE	SD D7	MS D3
SP5	XD ALE	SD CD#	MS D6
SP6	XD WE#	SD D6	MS D2
SP7	XD WP	SD D5	MS D0
SP8	XD D0	SD CLK	MS D4
SP9	XD D1	SD D4	MS D1
SP10	XD D2	SD D3	MS D5
SP11	XD D3	SD D2	MS BS
SP12	XD D4	SD D1	
SP13	XD D5	SD D0	
SP14	XD D6	SD D7	

Share Pin



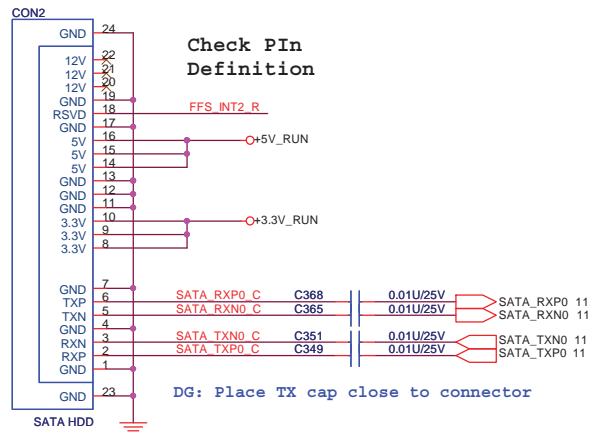
Cardreader	POP	NC
Inspiron	CON1	CON3
VOSTOR	CON3	CON1



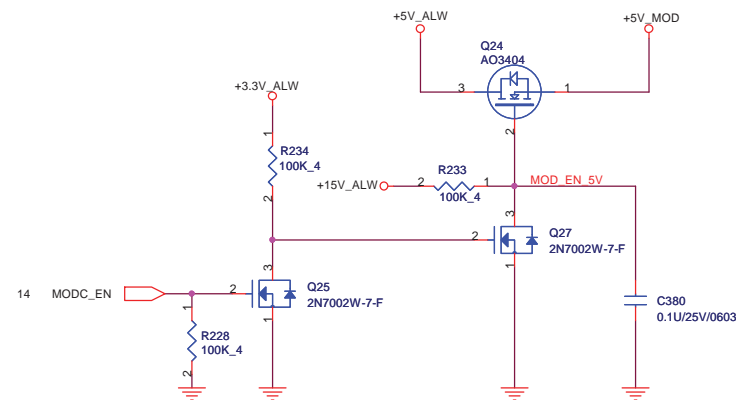
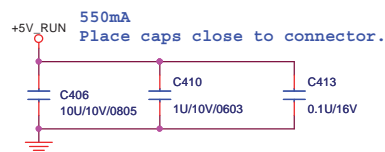
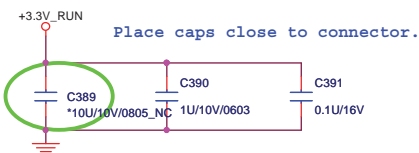
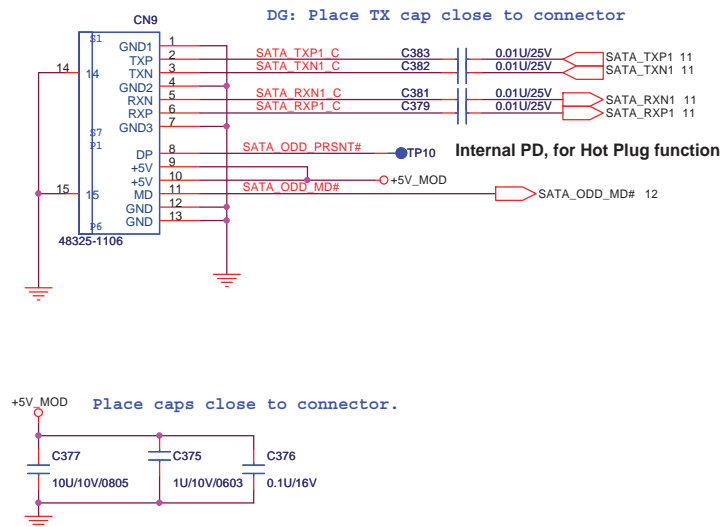
Quanta Computer Inc.

PROJECT : V02A/R01A

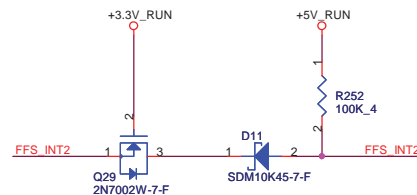
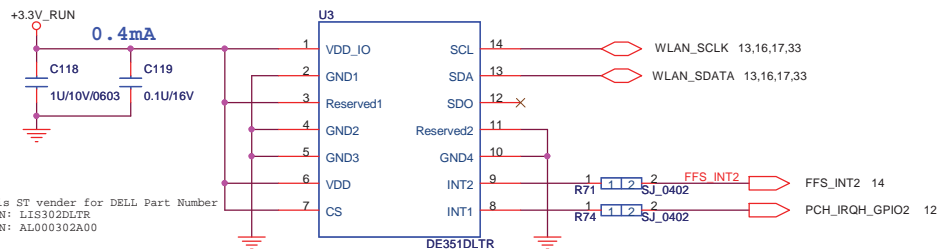
Size	Document Number	Rev
	Cardreader (RTS5128)	1A
Date	Wednesday, January 19, 2011	Sheet 30 of 61



ODD Connector



3-axis Fall Sensor (HDD data protector)



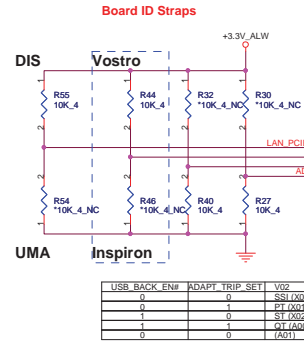
3-axis Fall Sensor	VOSTOR	Inspiron
U3, Q29, D11 R71, R74, R252 C118, C119	POP	NC



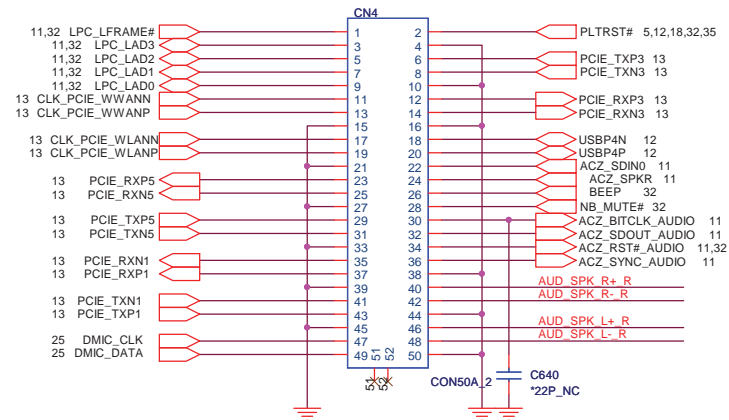
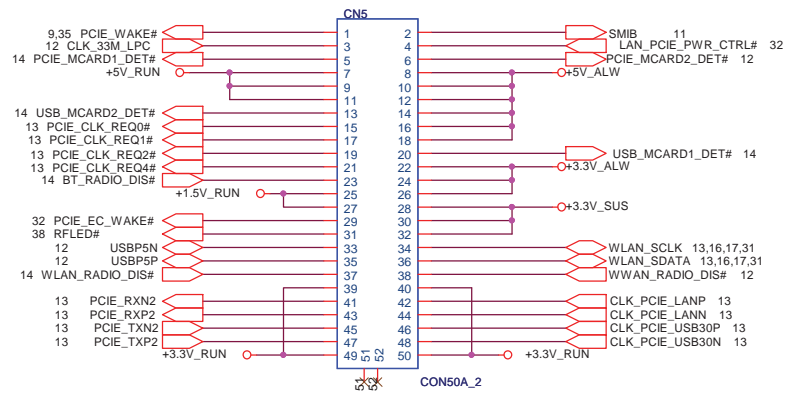
Quanta Computer Inc.

PROJECT : V02A/R01A

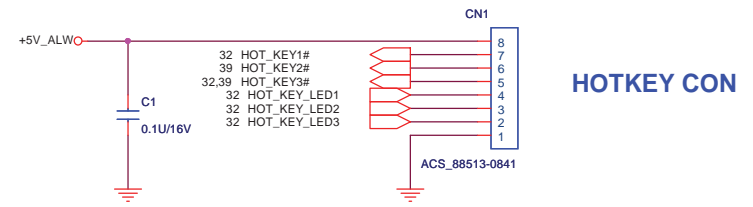
Size	Document Number	Rev
	SATA HDD/ODD	1A
Date:	Wednesday, January 19, 2011	Sheet 31 of 61

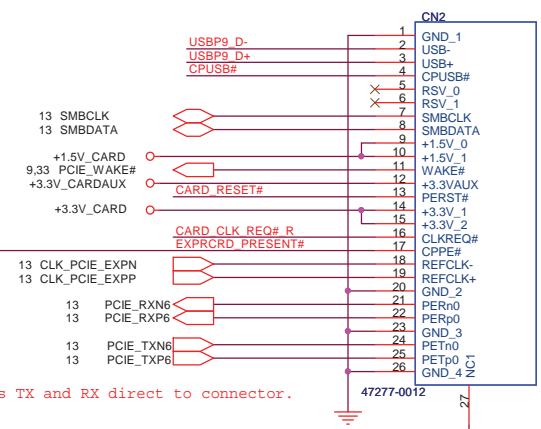
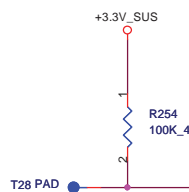
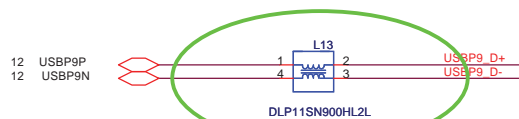


USB_BACK_EN#	ADAPT_TRIP_SET	V02
0	0	SSI (X00)
0	1	PT (X01)
1	0	ST (X02)
1	1	QT (A00)
0	0	(A01)



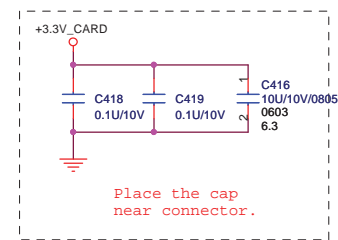
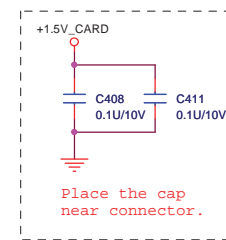
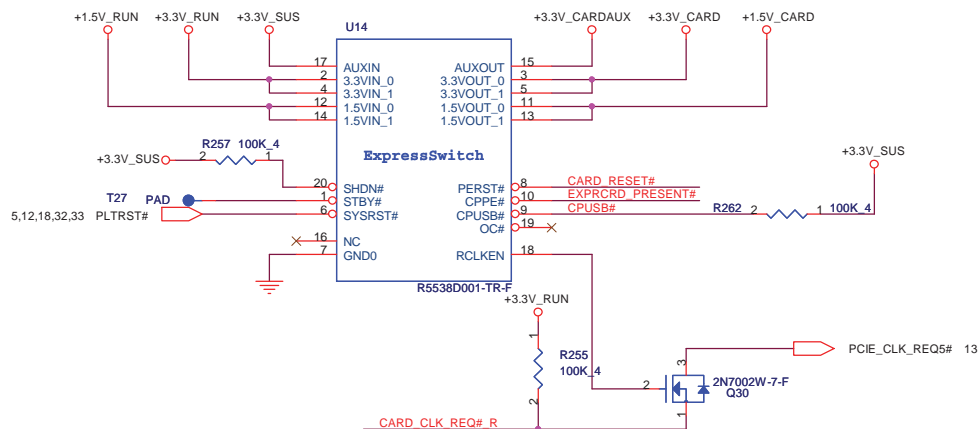
Int. Stereo Speakers
5V / 4 Ohm / 2W



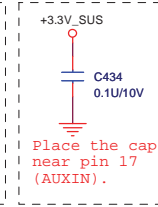
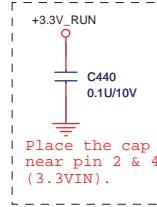
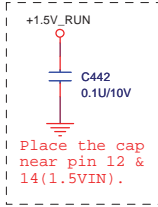
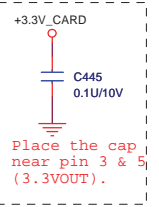


PCI-Express TX and RX direct to connector.

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



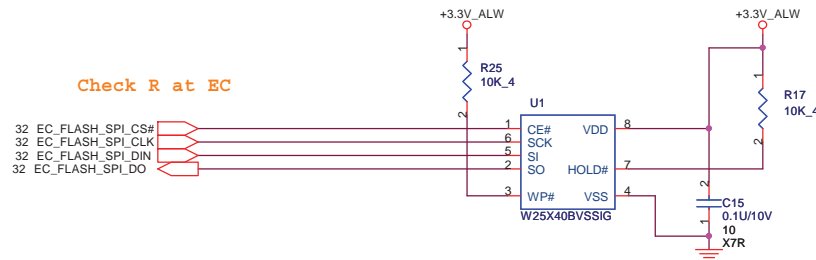
If close enough, could combine



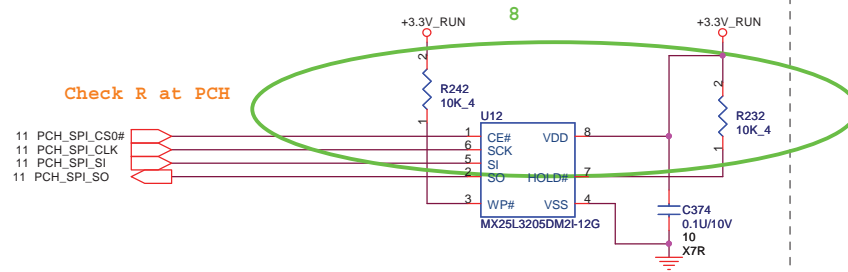
Quanta Computer Inc.
PROJECT : V02A/R01A

Size	Document Number	Rev
	LAN (RTL8111EL)	1A
Date:	Wednesday, January 19, 2011	Sheet 35 of 61

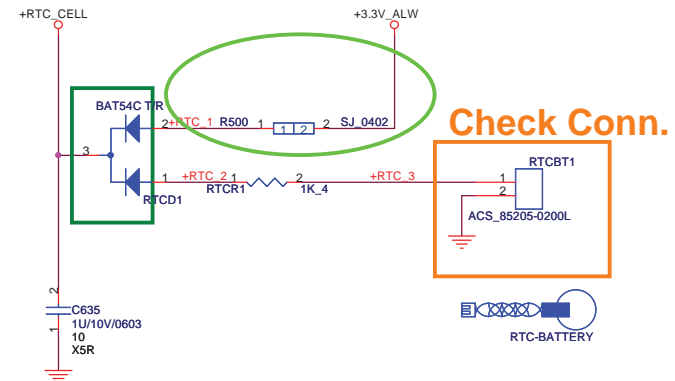
For EC 4Mbit (512K Byte)



For PCH 32Mbit (4M Byte)



RTC



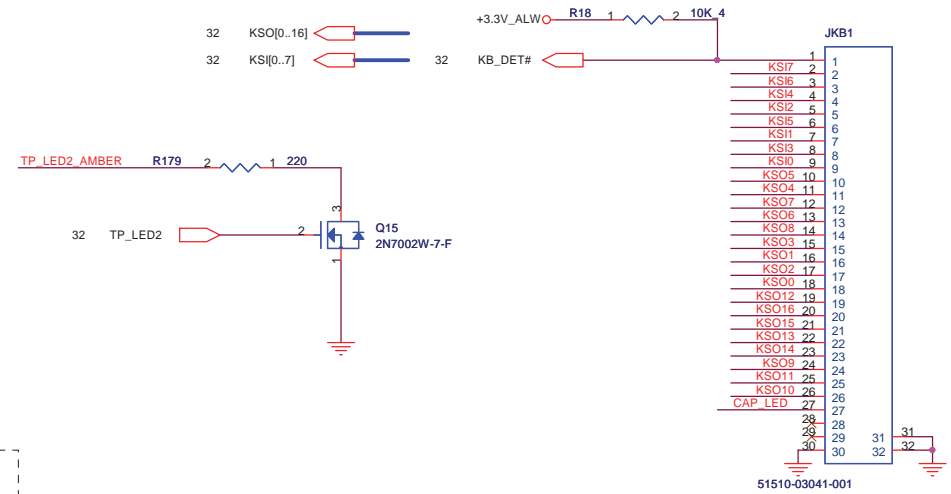
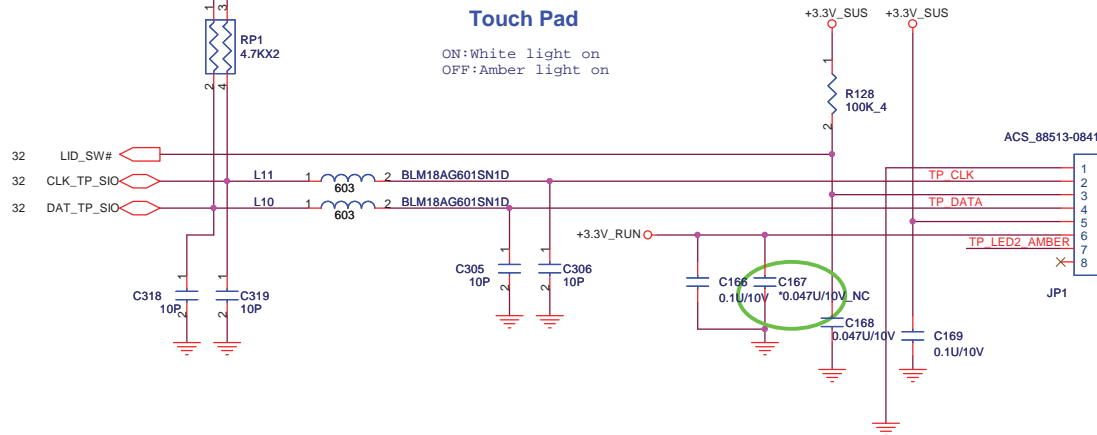
Double, 25'C, Vf=0.4V, If=25mA
one, 25'C, Vf=0.35V, If=15.8mA



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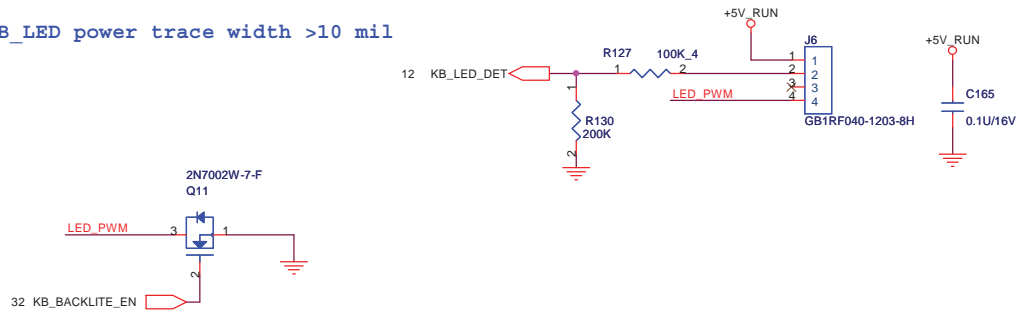
PROJECT : V02A/R01A

Size	Document Number	Rev
1A	FLASH / RTC	1A
Date:	Wednesday, January 19, 2011	Sheet 36 of 61

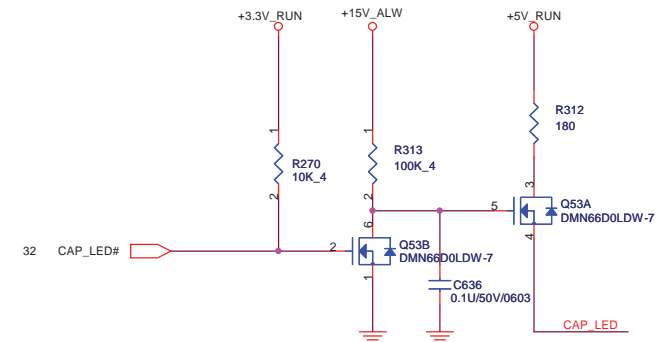
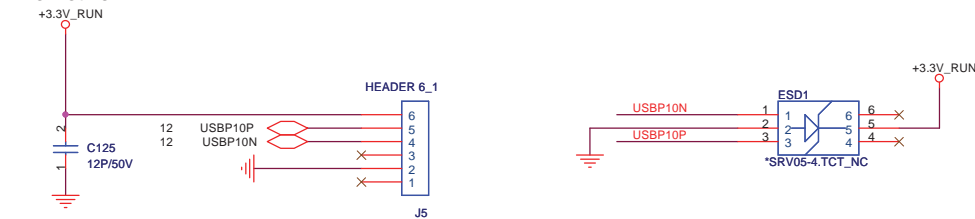


Key board illumination

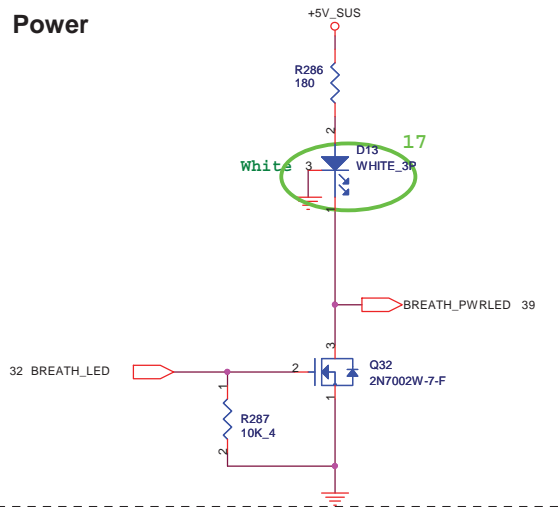
```
+KB_LED power trace width >10 mil
```



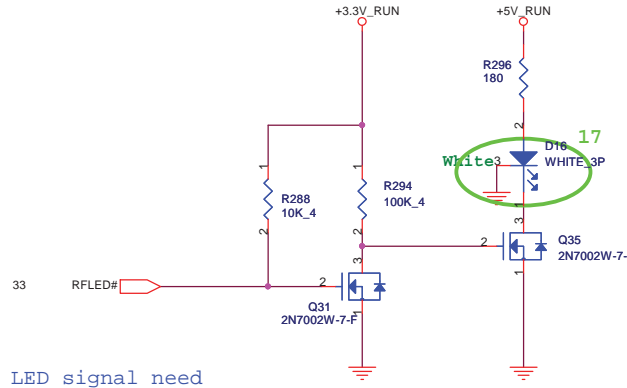
Biometric



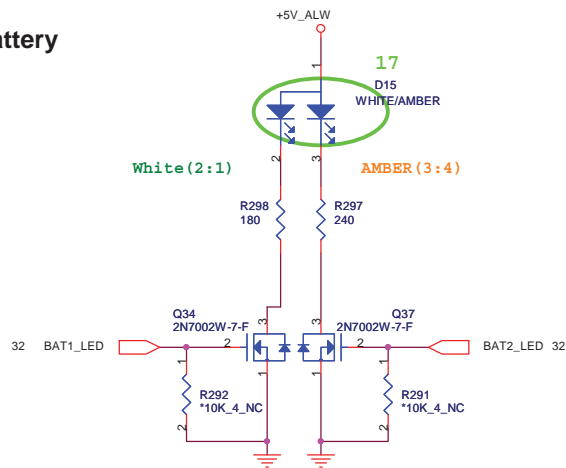
Power



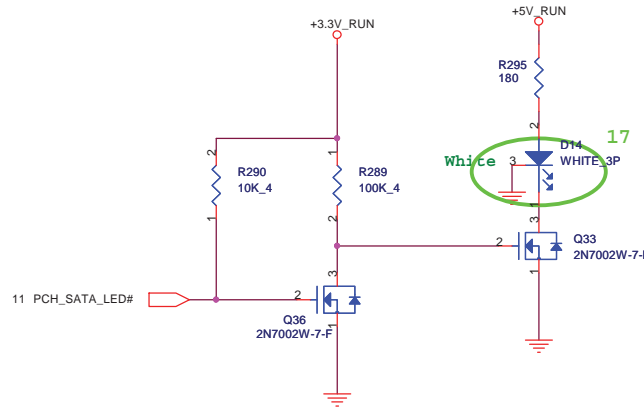
Bluetooth / WLAN on/off LED



Battery



HDD activity LED.

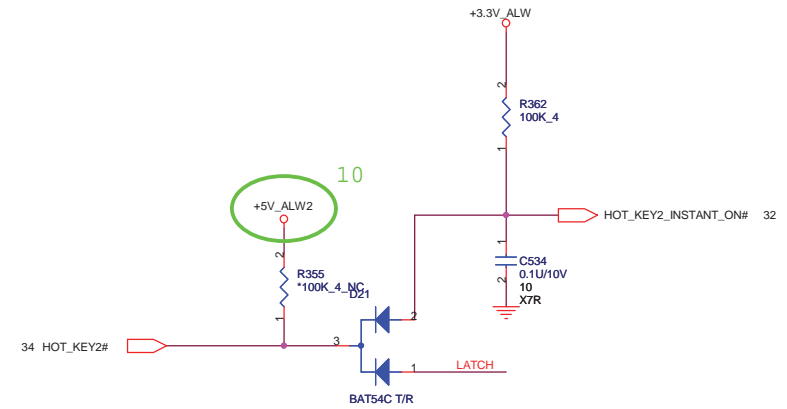
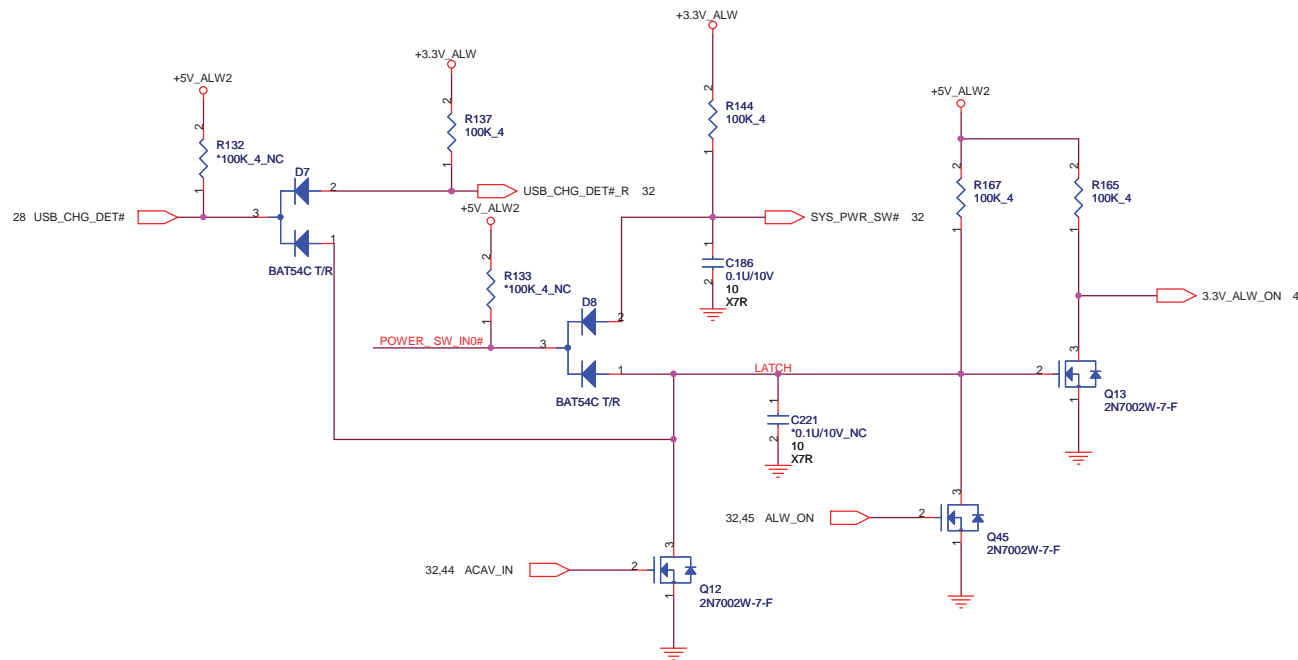


VOSTOR	R286, R295, R296, R298	R297
	180 ohm PN:CS11802JB15	240 ohm PN:CS12402JB13
Inspiron	R286, R295, R296, R298	R297
	390 ohm PN:CS13902JB14	330 ohm PN:CS13302JB21



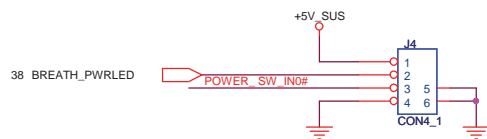
Quanta Computer Inc.
PROJECT : V02A/RO1A

3VALW ON POWER LOGIC

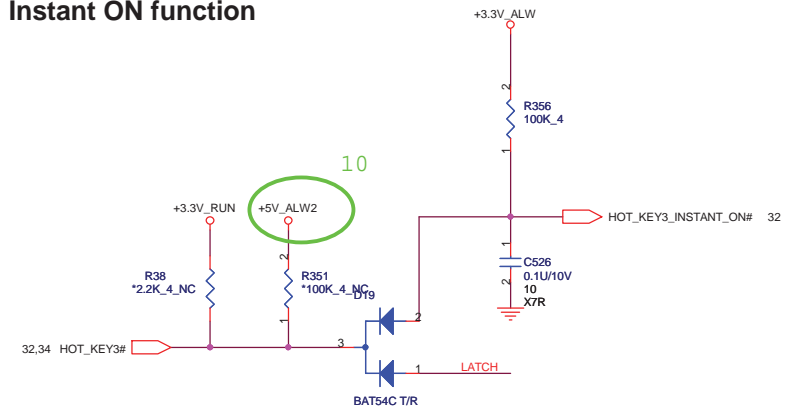


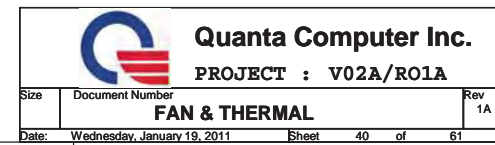
Vostro pop D19,C526,R356 depop R38,R39
Inspiron depop D19,C526,R356 pop R38,R39

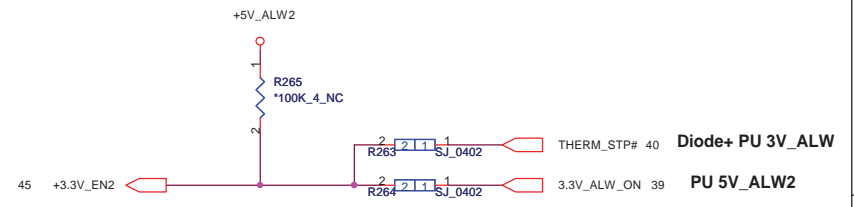
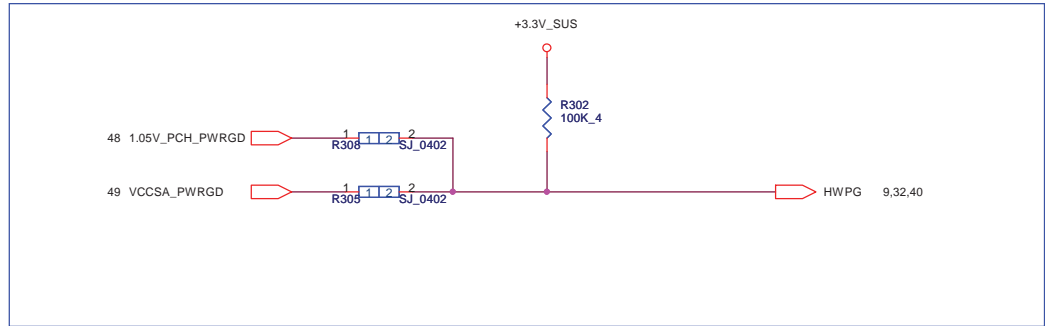
PWR button board

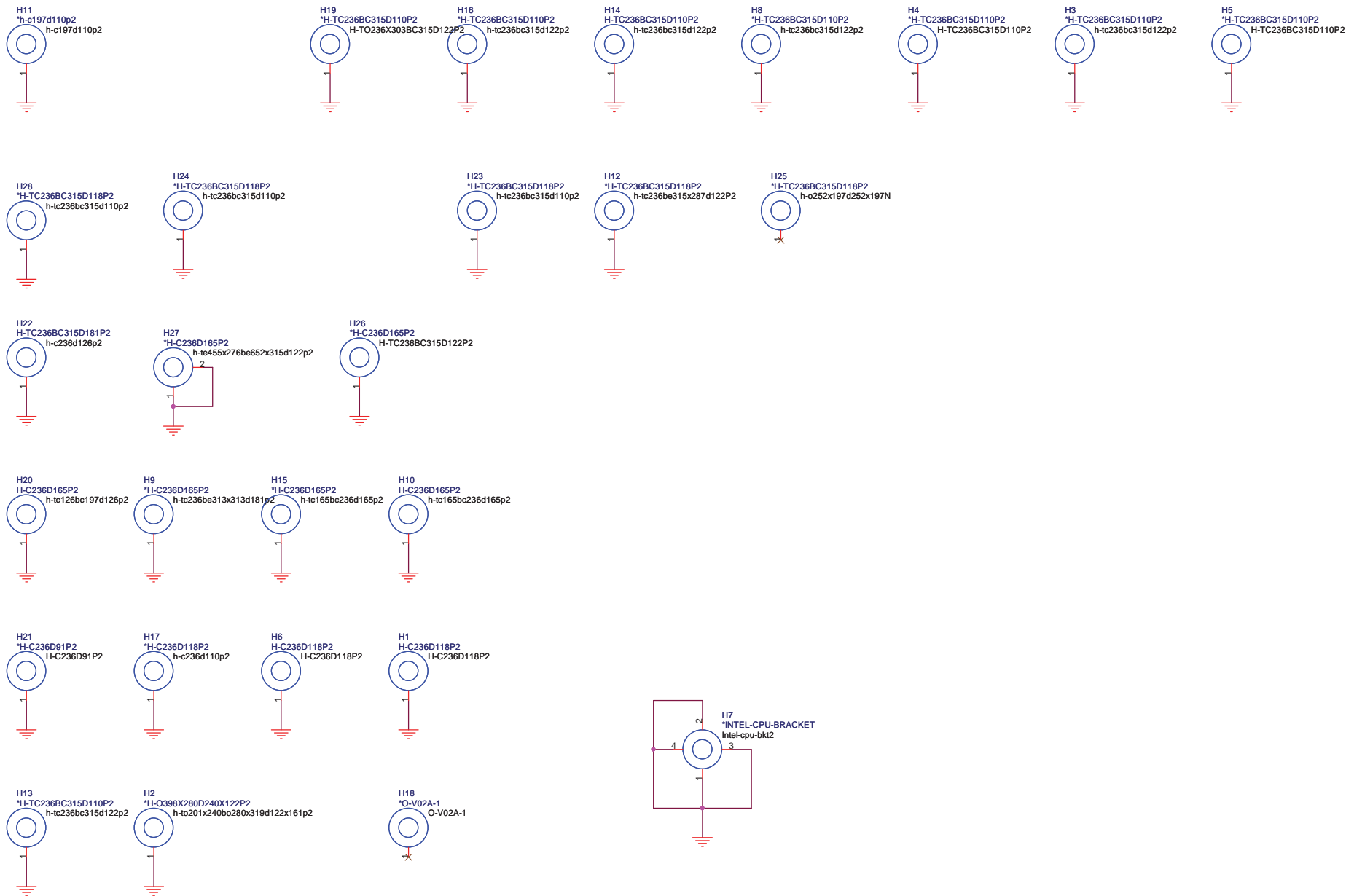


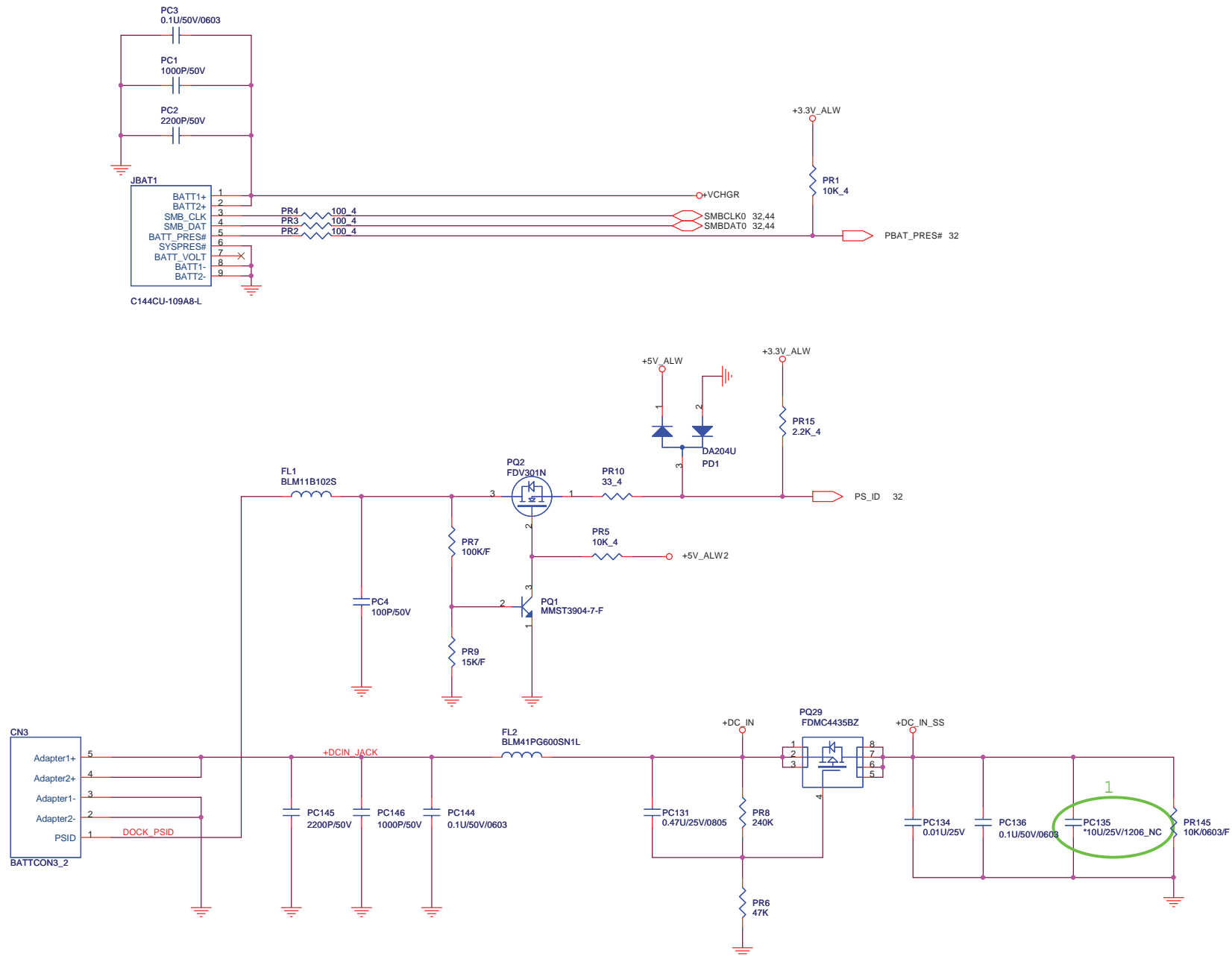
Instant ON function

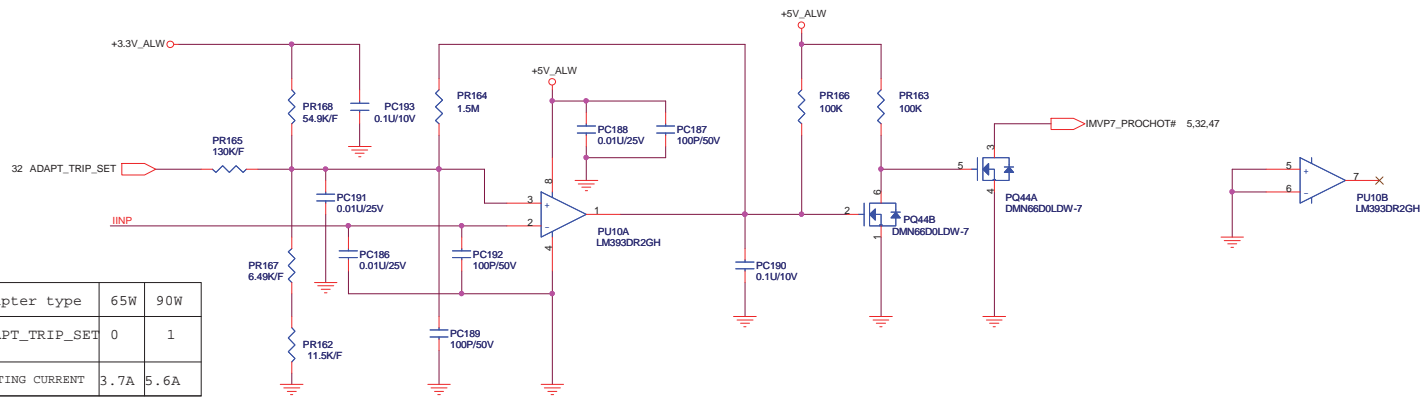
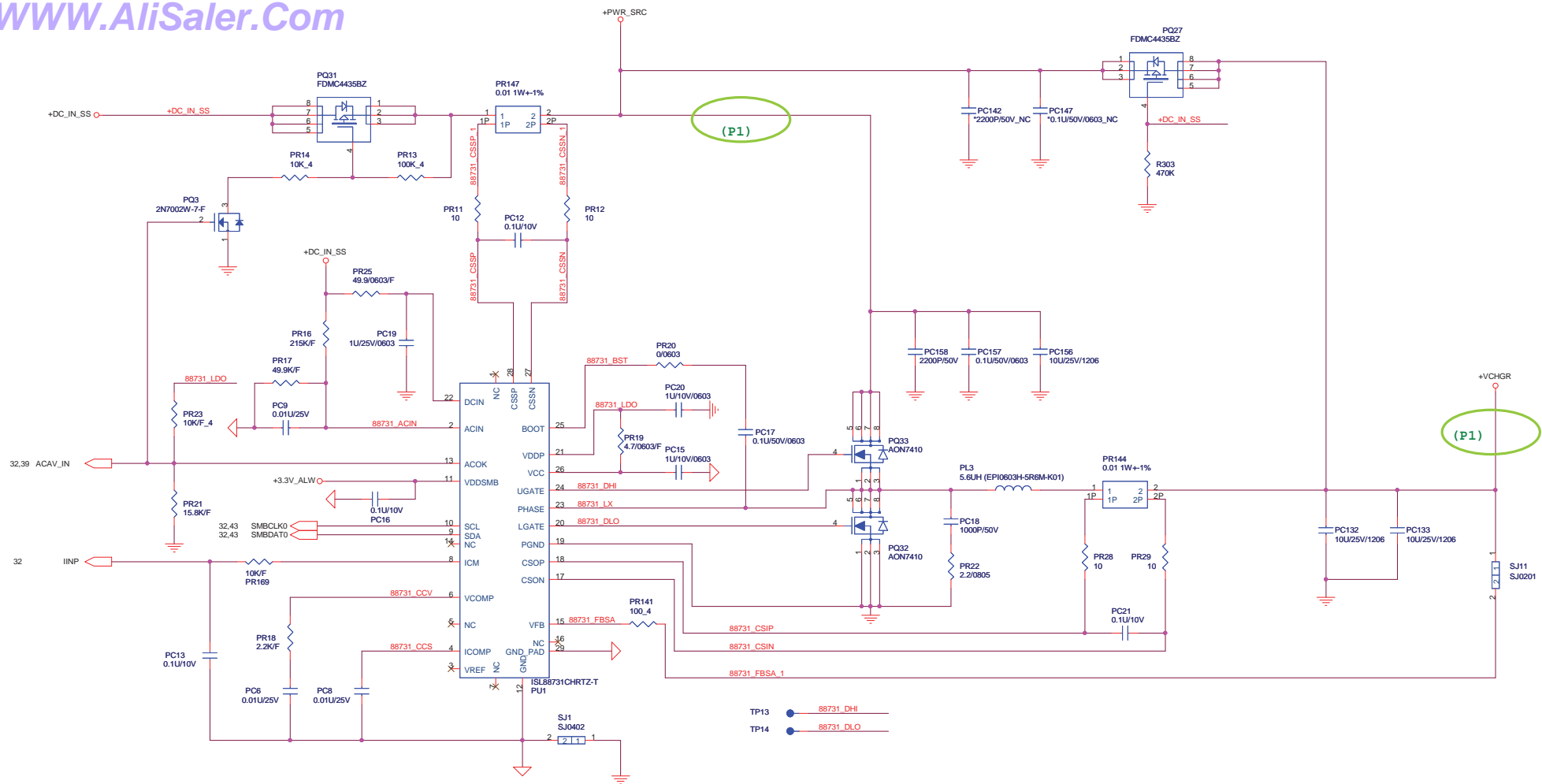


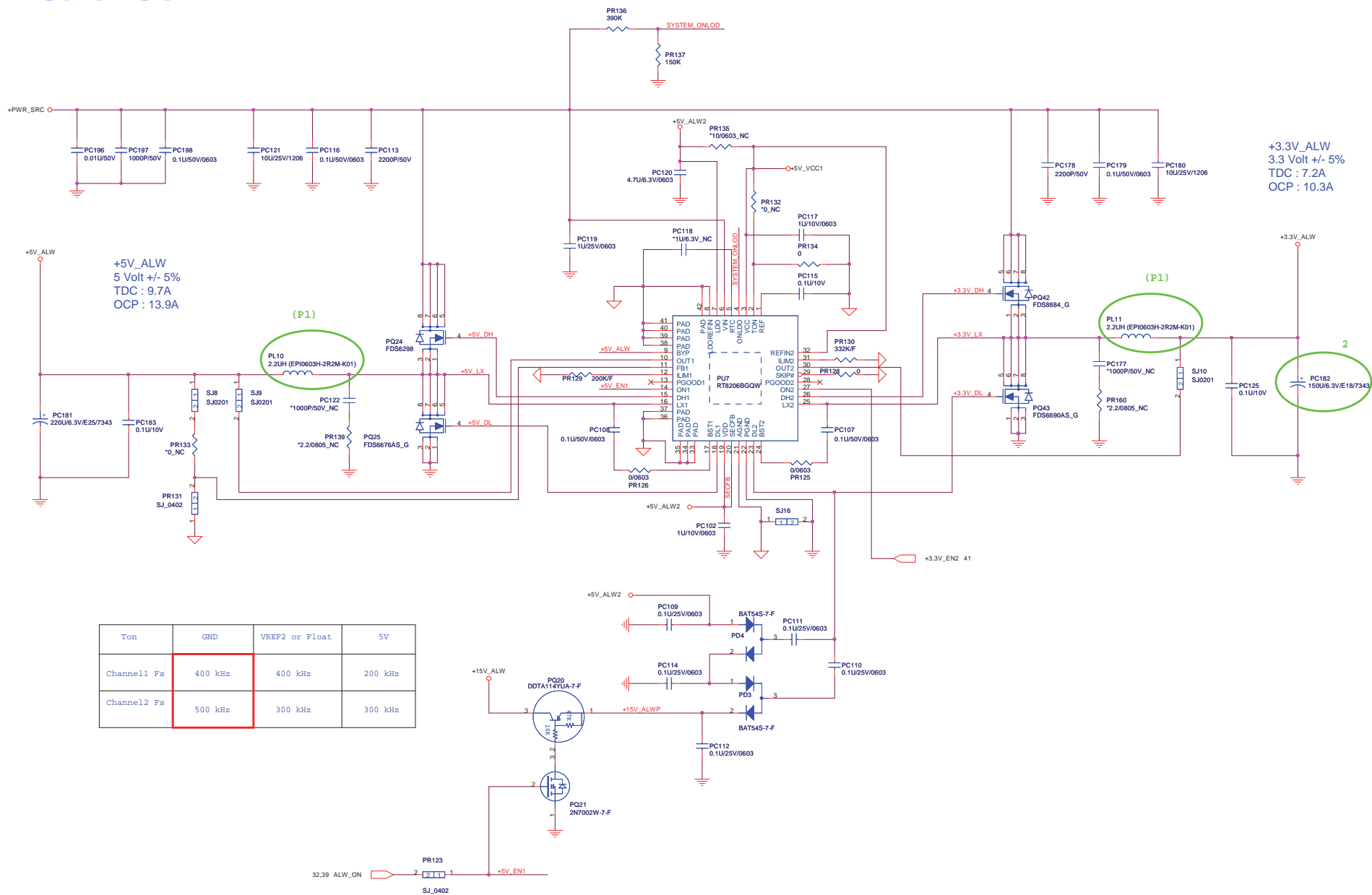










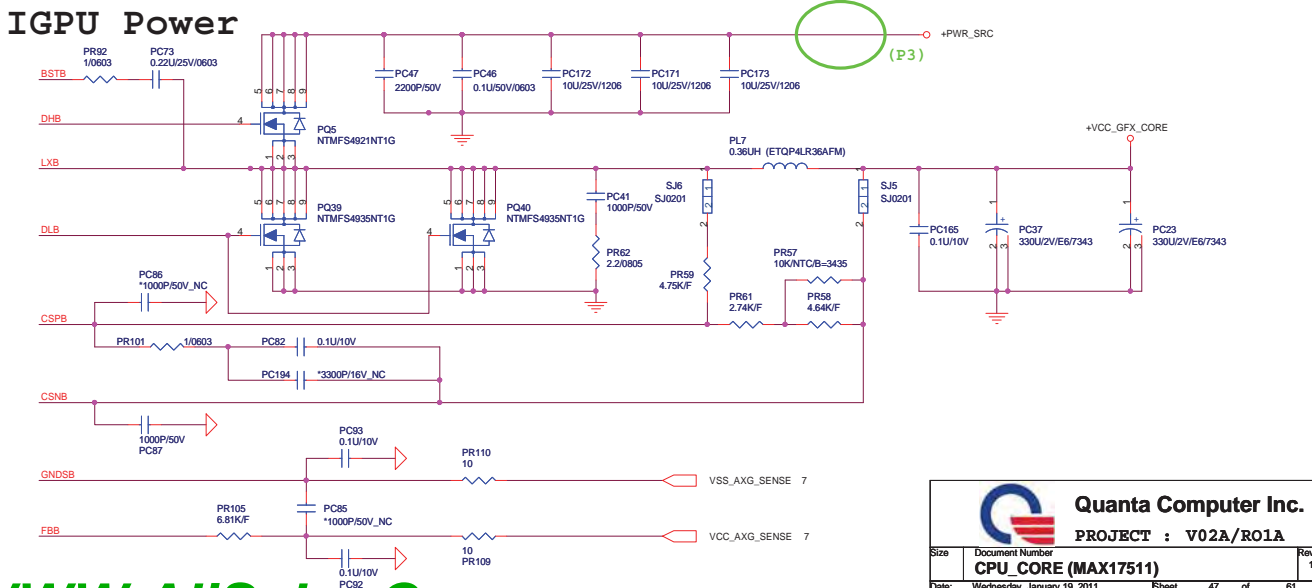
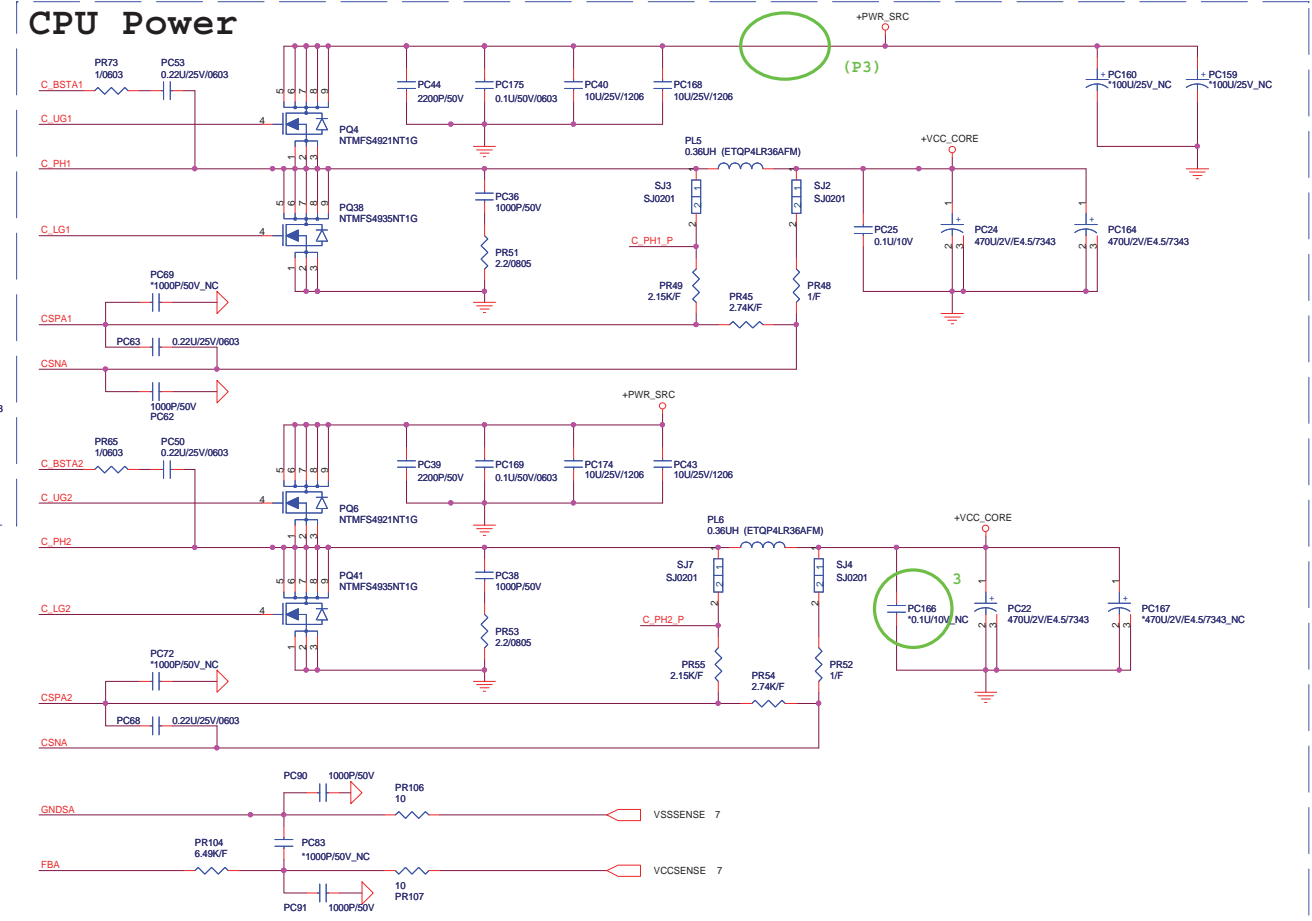


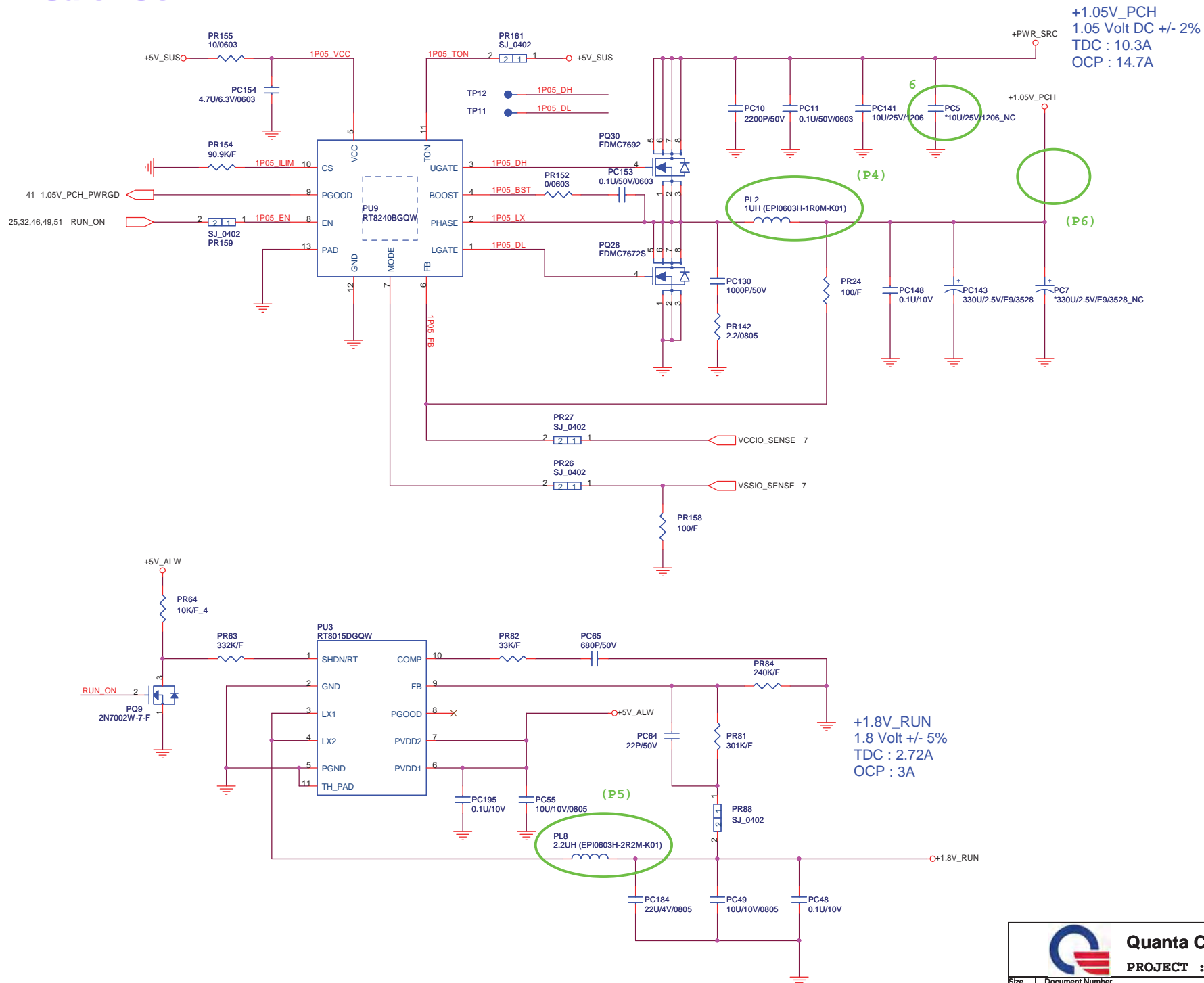


VDDQ and VTT discharge control

VDDQ output voltage selection

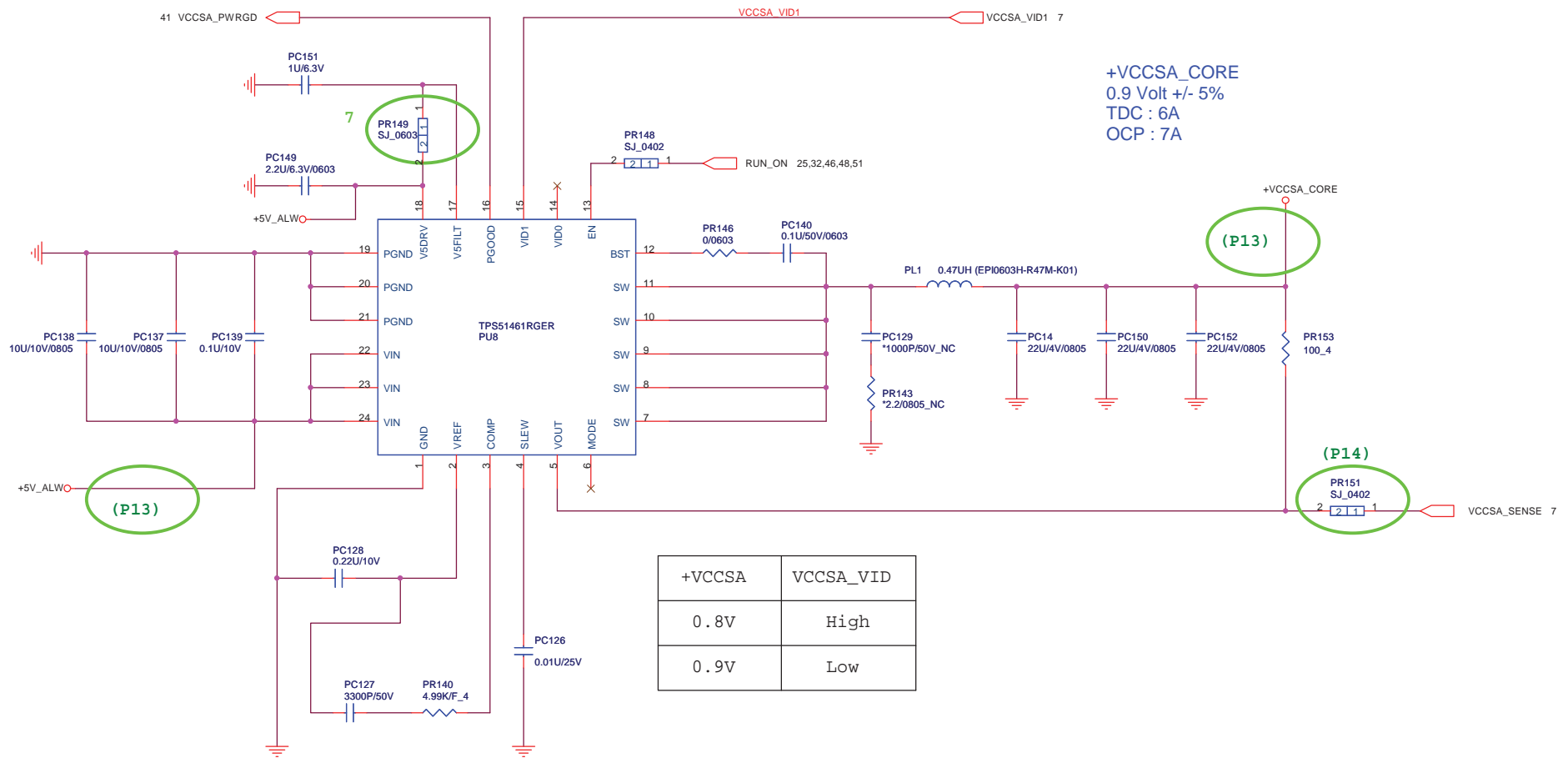
VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

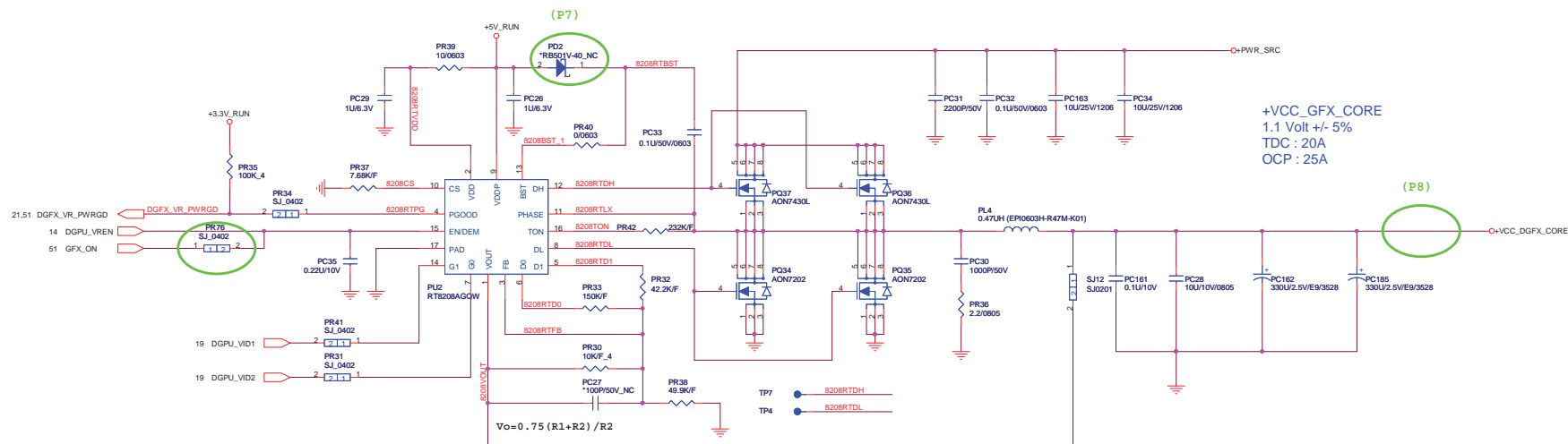




Quanta Computer Inc.
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Robson_XT

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
HIGH	HIGH	1.12V
Setting		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS34992FB10	49.9K
PR33	CS41502FB18	150K
PR32	CS34222FB00	44.2K

Whistler_LP

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	0.9V
HIGH	HIGH	1.0V
Setting		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS37502FB12	75K
PR33	CS41502FB18	150K
PR32	CS37502FB12	75K

Seymour_XT

DGPU_VID2	DGPU_VID1	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	0.9V
LOW	HIGH	1.0V
HIGH	HIGH	1.1V
Setting		
Location	Part No.	Value
PR30	CS31002FB26	10K
PR38	CS37502FB12	75K
PR33	CS41072FB11	107K
PR32	CS34122FB19	41.2K

